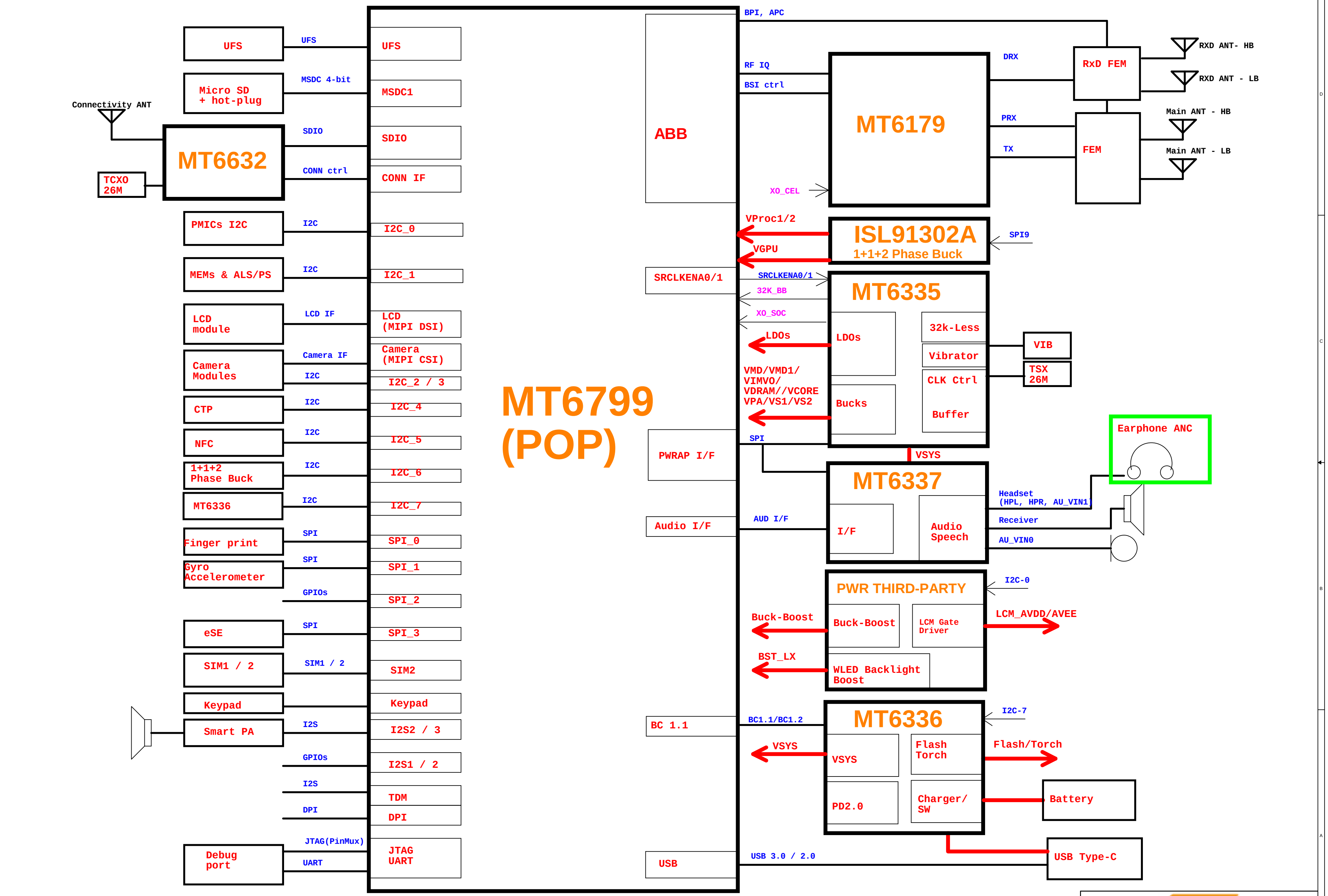

MEDIATEK

Title: 01_Block_Diagram

Size: C

MTK Confidential

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I2C	Function	I2C Spec.[1]	I2C Slave Address (7-bit mode)
I2C-0 *[2]	LCM Gate Driver	400 Kbps	RT4801A / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
	LPDDR4X Buck	400 Kbps	RT5738AWSC / LPDDR4X Buck I2C address: 0X50 (Write:0xA0, Read:0xA1)
	Speaker Amp.	400 Kbps	RT5509 / Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69) when ADS1/2 = GND
I2C-1 *[2]	M Sensor	400 Kbps	AK09915 / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)
	Baro Sensor	400 Kbps	BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	ALPS	400 Kbps	CM36558 / ALPS I2C address: 0X51 (Write:0xA2, Read:0xA3)
I2C-2	Rear camera	400 Kbps	IMX338 / Rear camera I2C address: 0X1A (Write:0x34, Read:0x35)
	Rear camera's AF	400 Kbps	AK7371 / AF driver I2C address: 0X0C (Write:0x18 Read:0x19)
I2C-3	2nd rear camera	400 Kbps	IMX258 / Front camera I2C address:0X10 (Write:0x20, Read:0x21)
	Front camera	400 Kbps	S5K4E6 / Front camera I2C address: 0X35 (Write:0x6A, Read:0x6B)
	2nd rear camera' s AF	400 Kbps	AK7371 / AF driver I2C address: 0X0C (Write:0x18 Read:0x19)
I2C-4	CTP	400 Kbps	GT1511 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0X14 (Write:0x28, Read:0x29)
I2C-5	NFC	1.3Mbps	MT6605 / NFC I2C address: 0X28 (Write:0x50, Read:0x51)
I2C-6	VPROC buck	3.4 Mbps	ISL91302 / 4-Phase Buck I2C address: 0X1E (Write:0x3C, Read:0x3D)
I2C-7	MT6336	3.4 Mbps	MT6336 / I2C address: 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59

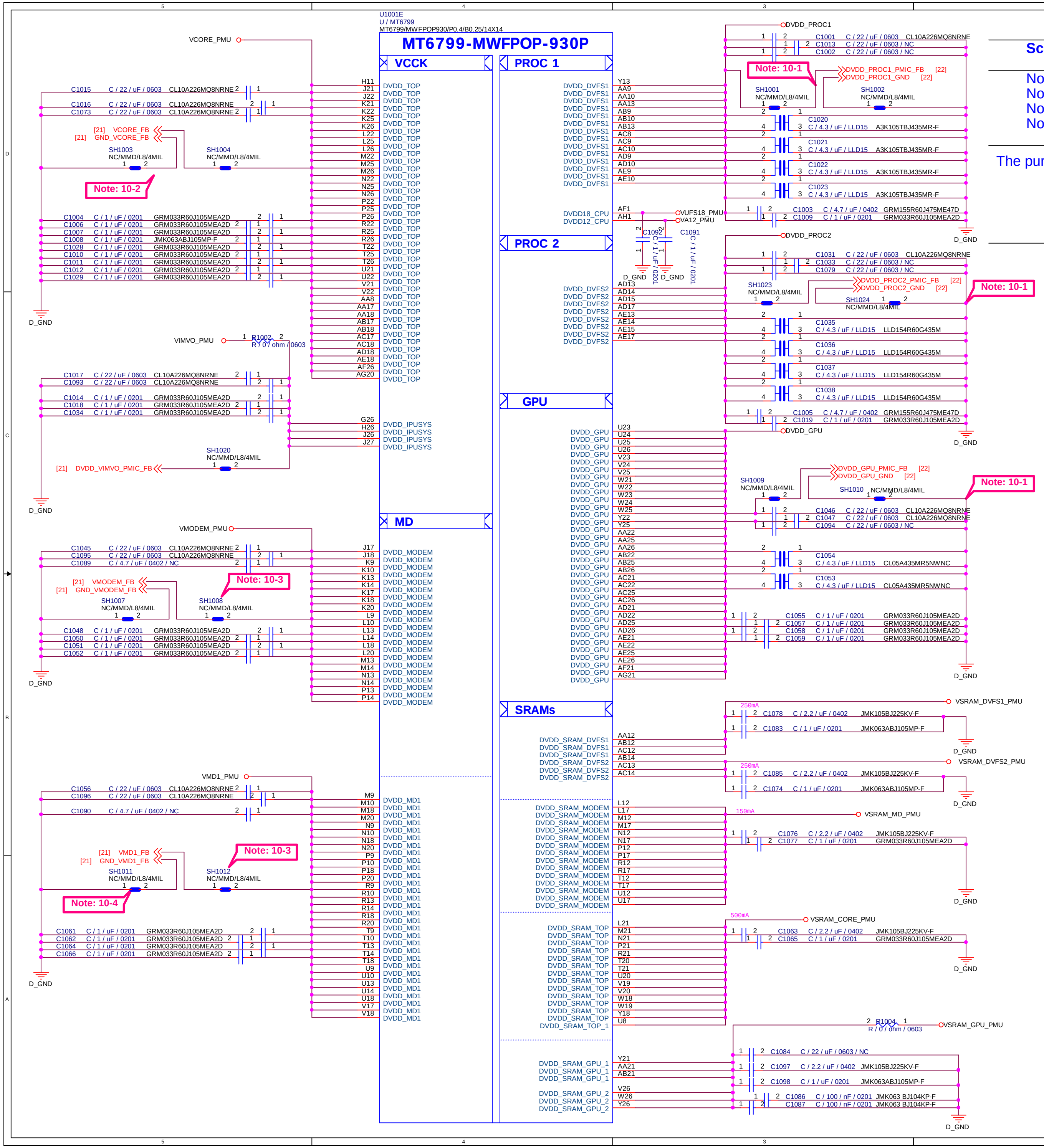
Note 1: I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Note 2: For MEMs sensor/sensor hub application, these I2C slave devices must be connected to I2C0 or I2C-1.

Date	Category	Item
2016.06.07 (V0.1)	General	Preliminary release
2016.06.27 (V0.2)	Page 10	[POWER] Saperated U1001 DVDD_SRAM_DVFS1/DVDD_SRAM_DVFS2 and supplied by VSRAM_DVFS1_PMU/VSRAM_DVFS2_PMU
	Page 10	[POWER] Added C1083 C / 1 / uF / 0201 and C1085 C / 2.2 / uF / 0402 for stability
	Page 10	[POWER] Added C1084 C / 22 / uF / 0603 / NC for stability
	Page 10	[POWER] DVDD_SRAM_PMU2 tied togather with DVDD_SRAM_PMU1 using same power source VSRAM_GPU_PMU
	Page 10	[POWER] DVDD_DVFS2 connected to DVDD_PROC2 instead of DVDD_PROC1
	Page 12	[BB] C1210 changed from NC to C / 100 / pF / 0201
	Page 12	[BB] U1001 RFIC_ET0_P/RFIC_ET1_P and RFIC_ET0_N/RFIC_ET1_N tied together
	Page 20	[PMIC] Added C2024 "C / 1 / uF / 0201 / NC", R2031 R2032 R033 R2035 "R / 0 / Ohm / 0201", R2034 "R / 0 / Ohm / 0201 / NC" for TSX/TCXO option
	Page 21	[PMIC] Removed U2002 RT4805A, changed C2171 to NC
	Page 22	[PMIC] U2202 changed to ISL91302AIIZ-T
	Page 23	[PMIC] Removed instant charger U2307
	Page 24	[PMIC] U2410 changed to RT6158WSC
	Page 28	[Audio] Added C2821 C2822 "C / 22 / nF / 0201", R2814 R2815 "R / 64.9 / ohm / 0201" to improve THD+N
	Page 32	[RF] U3239 changed to SAFEA1G90MA0F0A
	Page 50	[Consys] C5023 changed from 10uF to 22uF
	Page 51	[Consys] Added R5117 R5118 "R / 0 / Ohm / 0201" L5131 L5132 L5133 L5134 "L / nH / 0201 / NC" for notch filter
2016.07.19 (V0.3)	Page 2	[BB] RT5509 I2C slave address changed from 0x31 to 0x34
	Page 10	[BB] C1035, C1036, C1037, C1038 changed to "LLD154R60G435M"
	Page 11	[BB] R1116 changed to installed, R1115 changed to NC
	Page 21	[POWER] Removed C2135 C2136 C2157 C2158 C2159
	Page 24	[POWER] C2420 changed to "C / 10 / uF / 0603", L2402 L2403 changed to "PL / 0.33 / uH / 2016" [POWER] U2408 changed from FAN53528EUC48X to FAN53528GUC48X; U2410 changed from RT6185WSC to RT6158H
	Page 31	[RF] R3112, R3119 changed to "R / 37.4 / ohm / 0201" [RF] R3113, R3117, R3122, R3123 changed to "R / 150 / ohm / 0201"
	Page 32	[RF] Swap MIPI3 and MIPI5 [RF] Band 39 satellite PA VCC1 connected to VBAT; Band 39 satellite PA C3234 changed to "C / 470 / nF / 0201" [RF] Band 42 satellite PA C3229 C3208 changed to "C / 470 / nF / 0201" [RF] C3222, C3223 changed to "C / 1 / uF / 0201"; C3504 changed to "C / 47 / nF / 0201"
	Page 50	[Consys] Removed R5020, R5023, R5025, R5033, R5037, R5042, R5035, R5039, R5043
	Page 51	[Consys] Removed L5117, C5116, C5177, C5178, C5126 L5137, C5104, R5117, L5131, L5132, R5118, L5134, L5133, R5115, L5106, L5107, R5112, L5102 and L5103 [Consys] U5102, U5109 changed to "885171"
	Page 52	[NFC] Added C5246 "C / 12 / pF / 0201/ NC"

Date	Category	Item
2016.08.18 (V0.4)	Page 10	[BB] Added C1086 C1087 "C / 100 / nF / 0201" [BB] U1002 part number is H9HKNNNEBMAUCR
	Page 11	[BB] Added C1170 C1171 "C / 1 / uF / 0201"
	Page 12	[BB] R1204 changed to "R / 4.7 / K / 0402" from NC R1203 changed to NC from "R / 4.7 / K / 0402"
	Page 12	[BB] Removed C1201 C1202 "C / 1 / uF / 0201"
	Page 12	[BB] Removed C1203 C1204 C1205 C1206 C1207 C1208 C1224 C1225 C1226 C1230 C1231 C1232 C1235 C1236 C1238 C1239 C1240 C1241 C1242 C1243 C1244 C1245 C1246 "C / 100 / nF / 0201"
	Page 23	[Charger] D2304 D2305 "D / NSR20F20NXT5G" changed to NC
	Page 24	[Power] U2406 changed from FAN53528BUC08X to RT5738AWSC [Power] U2408 changed from FAN53528GUC48X to RT5738CWSC [Power] C2415 changed from "C / 330 / nF / 0201" to R2442 "R / 0 / ohm / 0201"
	Page 52	[NFC] Reserved a PMOS between AS39230 RF_RX_CLK and MT6605 ANT_P [NFC] C5246 changed to "C / 12 / pF / 0201" from "C / 12 / pF / 0201/ NC"
2016.11.07 (V0.5)	Page 11	[BB] Ball AK1 changed connection from VSIM1_PMU to VUSB33_PMU and C1139 changed to "C / 1 / uF / 0201 / NC"
	Page 12	[BB] Added R1220 "R / 4.7 / K / 0402 / NC" and R1221 "R / 4.7 / K / 0402" which connected to VA12_PMU [BB] R1204 changed from "R / 4.7 / K / 0402" to NC [BB] C1247, C1248 moved to Page 11
	Page 12	[BB] Ball name of H15 was changed from AVDD09_A to DVDD_TOP Ball name of AF9 and AG9 were changed from AVDD09_B to DVDD_TOP Ball name of H20 and H24 were changed from AVDD09_C to DVDD_TOP Ball name of AF22 was changed from AVDD09_D to DVDD_TOP
	Page 13	[BB] Not support IC-USB, thus, ball USB_DP_P1 and USB_DM_P1 connected to ground [BB] Removed R1317 "R / 4.7 / K / 0201 / NC"
	Page 20	[Power] R2009 changed from NC to "R / 0 / ohm / 0201", R2036 changed from "R / 0 / ohm / 0201" to NC [Power] Removed R2030, R2031, R2032, R2033, R2034, R2035 "R / 0 / ohm / 0201" and C2024 "C / 1 / uF / 0201 / NC"
	Page 22	[Power] Removed R2203 and R2208; R2210 changed from "R / 10 / k / 0201" to NC
	Page 23	[Power] Removed R2333; C2301 must use 25V working voltage; Added test point TP2320, short pad SH2304
	Page 24	[Power] Removed external buck U2408 "U / RT5738CWSC"
	Page 28	[Audio] SH2801 changed from short pad to R2816 "R / 0 / ohm / 0201"
	Page 31	[RF] Updated U / MT6179 symbol of which is that added ball A1, A25, N1 and N25 respectively
	Page 32	[RF] Added C3264 and C3265 "C / 22 / pF / 0201"; Removed C3209, C3239, C3212, C3216, C3230 "C / 33 / pF / 0201"
	Page 33	[RF] Added C3379 "C / 22 / pF / 0201", C3399 changed from NC to "C / 22 / pF / 0201"; Removed C3314, C3316 "C / 33 / pF / 0201"
	Page 34	[RF] Added C3473 and C3474 "C / 22 / pF / 0201"
	Page 35	[RF] Added C3515 and C3516 "C / 22 / pF / 0201"
	Page 50	[Consys] Ball name of H14, H15, K14, K15, F13 and F14 were changed to NC; R5017 changed to NC
	Page 53	[NFC] NFC frontend was moved to page 53

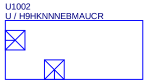
Date	Category	Item
2016.12.14 (V0.6)	Page 20	[PMIC] Removed C2009, C2010 "C / 22 / pF / 0201" and X2002
	Page 21	[PMIC] Removed power net VMIPI_PMU
	Page 32	[RF] Added R3203 "R / 0 / ohm / 0201" that connected to VIO18_PMU Changed VMIPI_PMU to VMIPI_RF
	Page 33	[RF] Changed power net name from VMIPI_PMU to VMIPI_RF
	Page 34	[RF] Changed power net name from VMIPI_PMU to VMIPI_RF
	Page 63	[Camera] Added R6311, R6312 "R / 0 / ohm / 0201" and added C6323, C6324 "C / 0201 / NC" to reduced EMI
2017.04.02 (V1.0)	Page 20	[PMIC] Removed R2018 "R / 0 / ohm / 0201" and C2018 "C / NC / 0201"
	Page 31	[RF] Removed R3124, R3125 "R / 0 / ohm / 0201"
	Page 50	[Consys] Removed C5048 "C / NC / nF / 0201"
	Page 60	[Audio] Replaced BEAD6015 with SH6003, replaced R6023 with SH6004
	Page 64	[Sensor] Removed R6446, R6448, R6449, R6452 and R6454 "R / 0 / ohm / 0201" Removed R6447, R6450, R6451 and R6453 "R / 0 / ohm / 0201 / NC" Added important design notices for magnetic sensor and accelerometer/gyroscope sensor



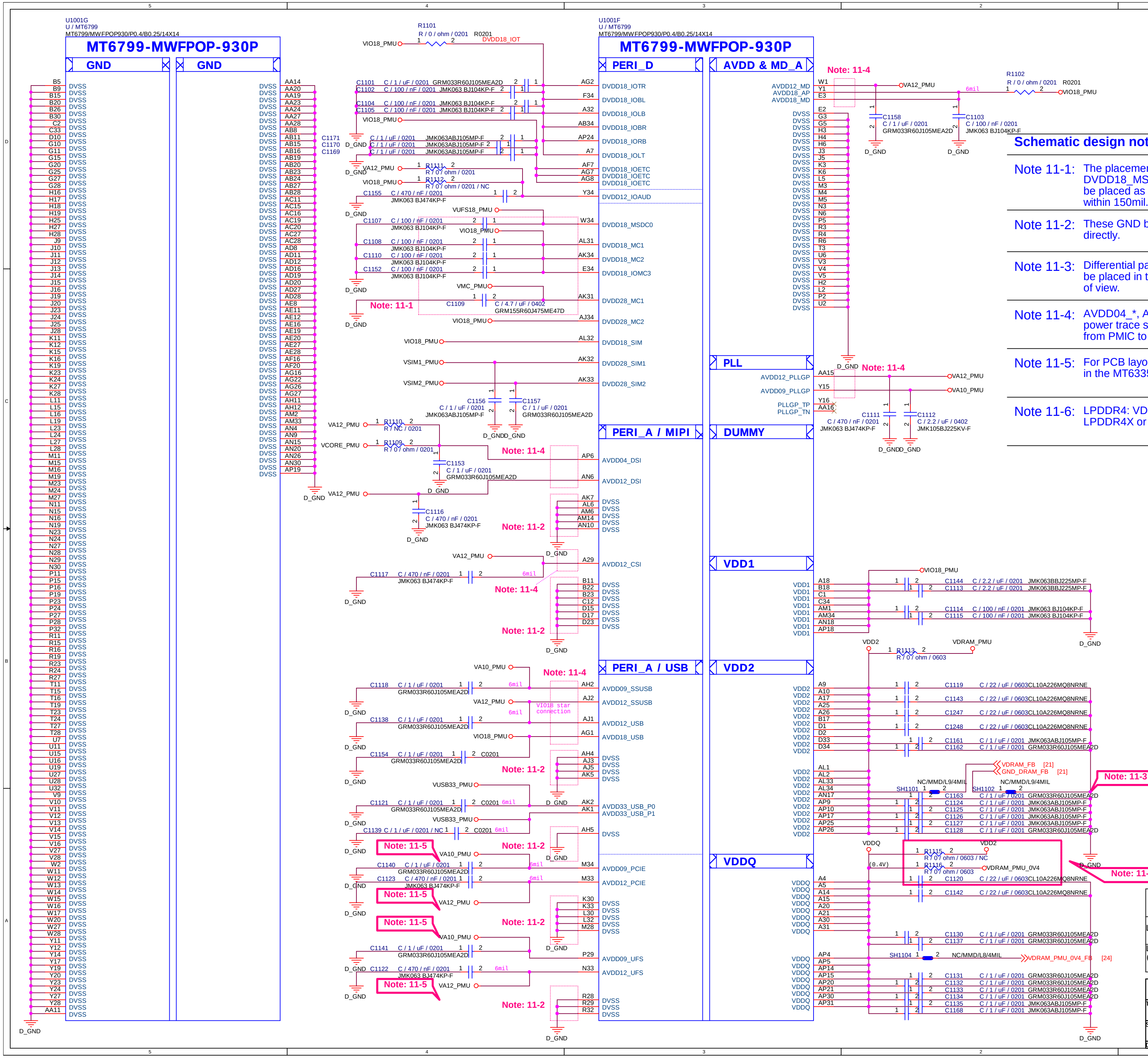
Schematic design notice of "10_BB_POWER_1" page.

Note 10-1:
Note 10-2: Differential pairs of buck's remote sense must be placed at PCB
Note 10-3: back side right beneath X30 chip.
Note 10-4:

The purpose of this symbol is used for including POP LPDDR4X in BOM.



Title	10_BB_POWER_1
Size C	MTK Confidential
Date:	Wednesday, April 26, 2017 — Sheet 10 of 99



Schematic design notice of "11_BB_POWER_2" page.

Note 11-1: The placement of power/de-coupling capacitors of DVDD18_MSDC0/1 &DVDD28_MSDC1should be placed as close to its power ball as possible within 150mil.

Note 11-2: These GND balls should be connected to main GND directly.

Note 11-3: Differential pair of VDRAM_PMU remote sense should be placed in the farest power plane from MT6335 point of view.

Note 11-4: AVDD04_*, AVDD09_*, AVDD12_*, and AVDD18_* power trace should be less than 0.1 ohm DC resistance from PMIC to AP

Note 11-5: For PCB layout, the star connection should be implemented in the MT6335's VA10 and VA12 output.

Note 11-6: LPDDR4: VDDQ=1.1V R1115:0ohm, R1116:NC
LPDDR4X or LPDDR4X+: VDDQ=0.6V or 0.4V, R1115:NC, R1116:0ohm

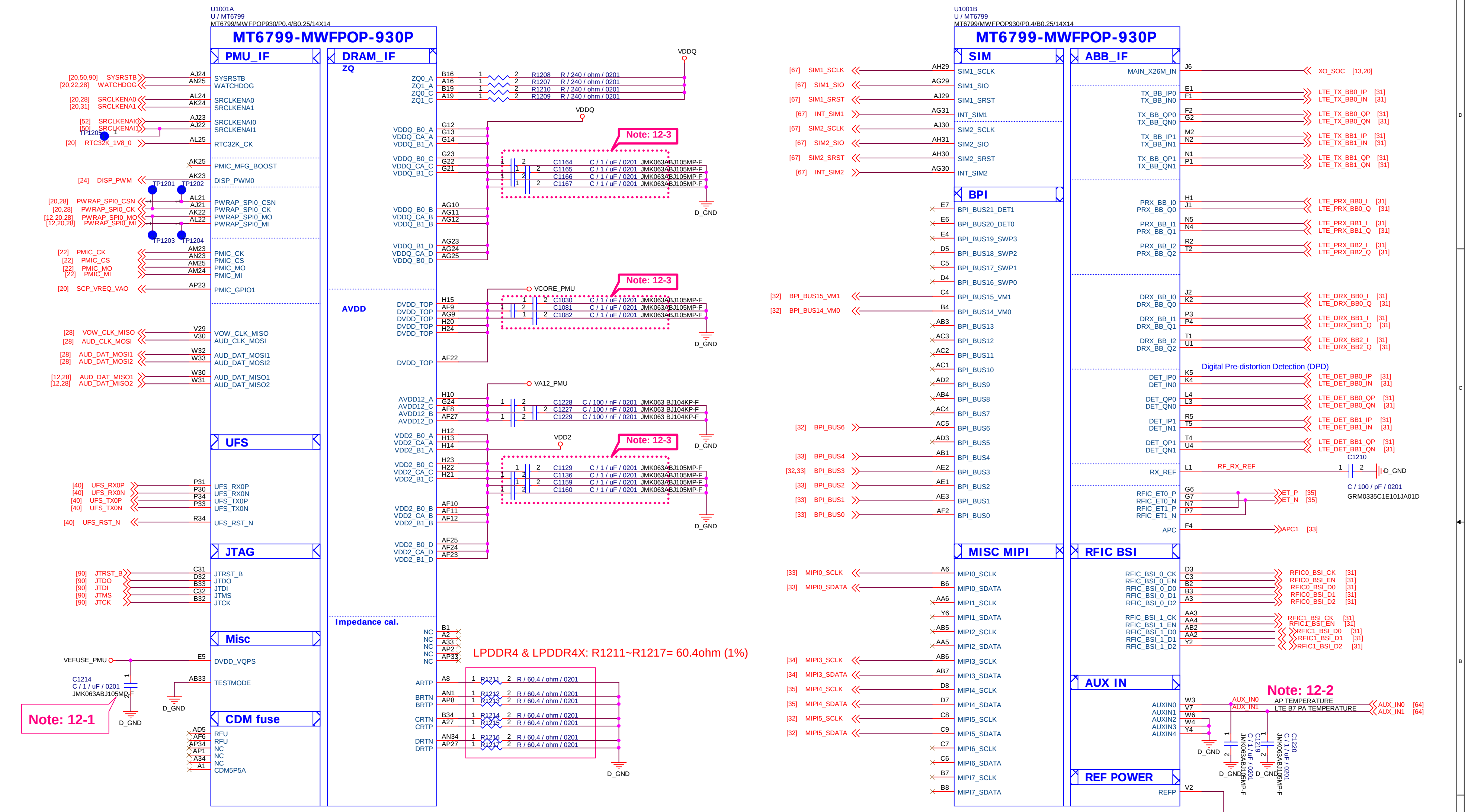
	R1115	R1116
LPDDR4 (VDDQ = 1.1V)	0 ohm	NC
LPDDR4X / LPDDR4X+ (VDDQ = 0.6V/0.4V)	NC	0 ohm

Title: 11_BB_POWER_2

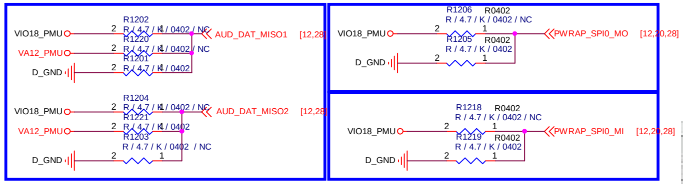
Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 11 of 99

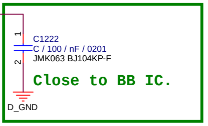


Trapping pin



Schematic design notice of "12_BB_1" page.

Note 12-1:	Apply 1.8V to DVDD_VQPS(E5) for eFuse programming.
Note 12-2:	To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible.Connect the unused AUX ADC input to GND.
Note 12-3:	Place on bottom layer and closed to SOC ball



	AP (TM) and MISO1 (T) both connect to VA12_PMU R1111 / FB2801	AP (TM) and MISO2 (T) both connect to VIO18_PMU R1112 / R2813
UFS BOOT / USB normal	R1221=4.7Kohm / R1201=4.7Kohm	R1204=4.7Kohm / R1201=4.7Kohm
eMMC BOOT / USB normal	[illegible]	[illegible]

		AP side			PMIC side			Function Description
Function name	Target reset level	AP PAD name	AP I/O	AP PU/PD	PMIC PAD name	PMIC I/O	PMIC PU/PD	
AP_USB_JTAG	LOW	[illegible]	Input	PD	AUD_DAT_MISO1(GPIO?)	Input	[illegible]	Ts1: USB JTAG via DP/DM Ts0: USB normal function
AP_BOOT_ROOM	LOW	[illegible]	Input	PD	AUD_DAT_MISO2 (GPIO?)	Input	[illegible]	Ts1: booting flow: UFS -> eMMC -> SPI_NOR -> SDMMC Ts0: booting flow: eMMC -> UFS -> SPI_NOR -> SDMMC
AP_IO_JTAG	LOW	PWRAP_SPI0_MI	Input	PD	SPI_MISO(GPIO?) SPI_MISO(GPIO?)	Input	[illegible]	Ts1: switch all IO_JTAG relative GPIO pinmux to IO_JTAG function Ts0: original behavior, IO_JTAG relative GPIO pinmux are controlled by gpio_mode registers
4266 DDR	Low	PWRAP_SPI0_MO	Input	PD	SPI_MOSI(GPIO?)	Input	PD	

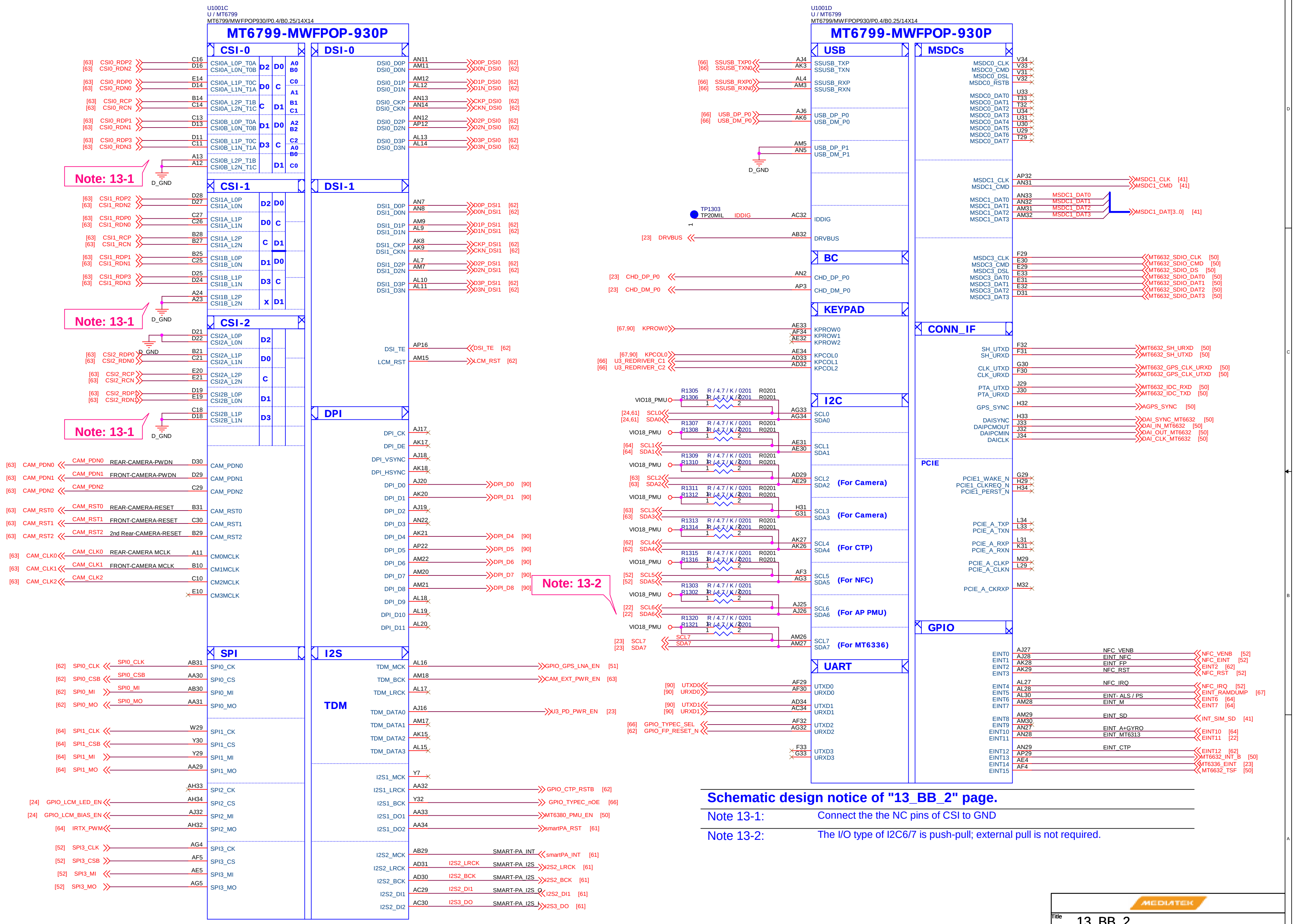
MEDIATEK

Title: 12_BB_1

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 | Sheet 12 of 99



Schematic design notice of "13_BB_2" page.

Note 13-1:	Connect the the NC pins of CSI to GND
Note 13-2:	The I/O type of I2C6/7 is push-pull; external pull is not required.

MEDIATEK

Title	13_BB_2
Size C	MTK Confidential
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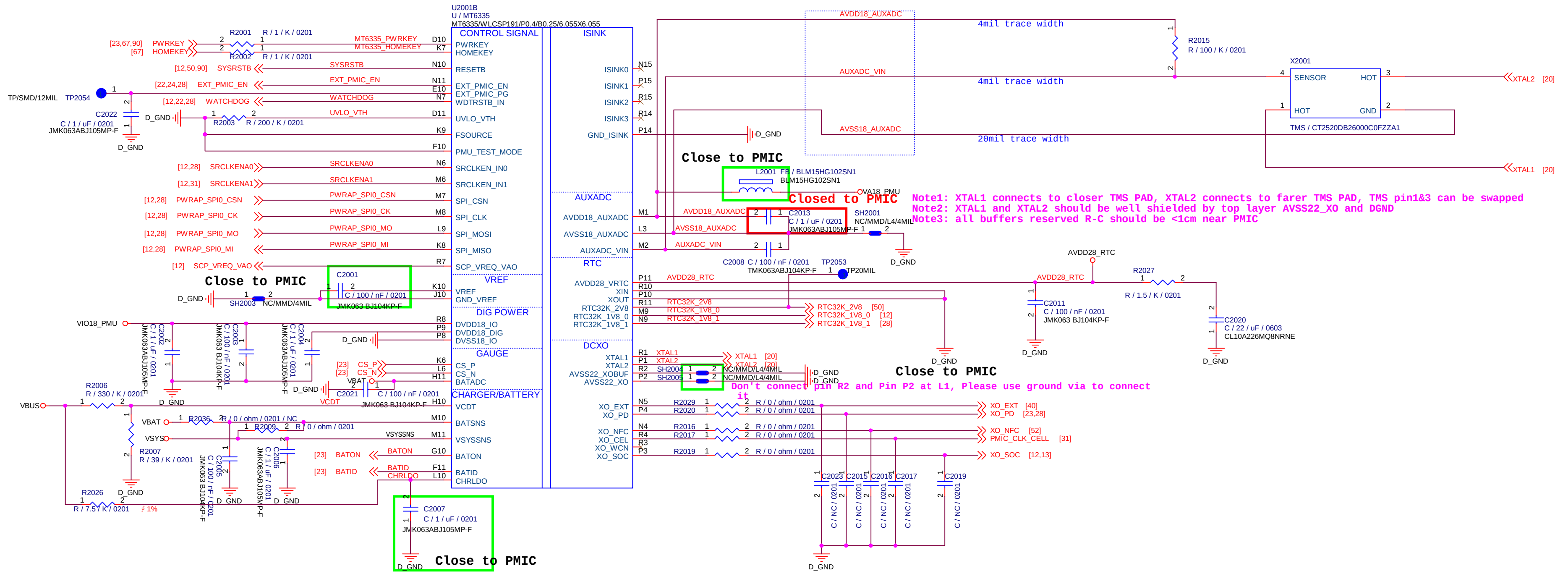
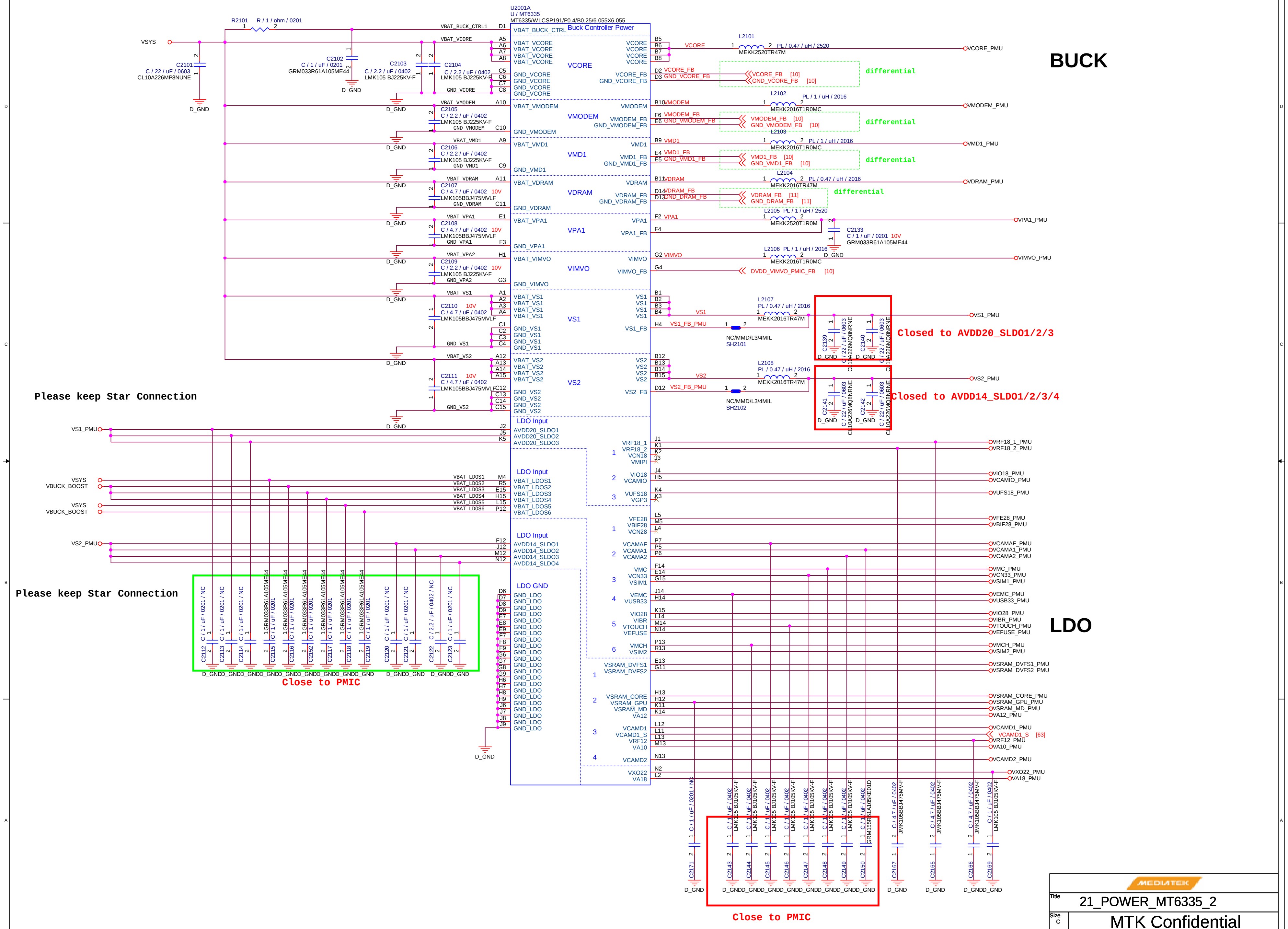


Title: 20_POWER_MT6335_1

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 20 of 99



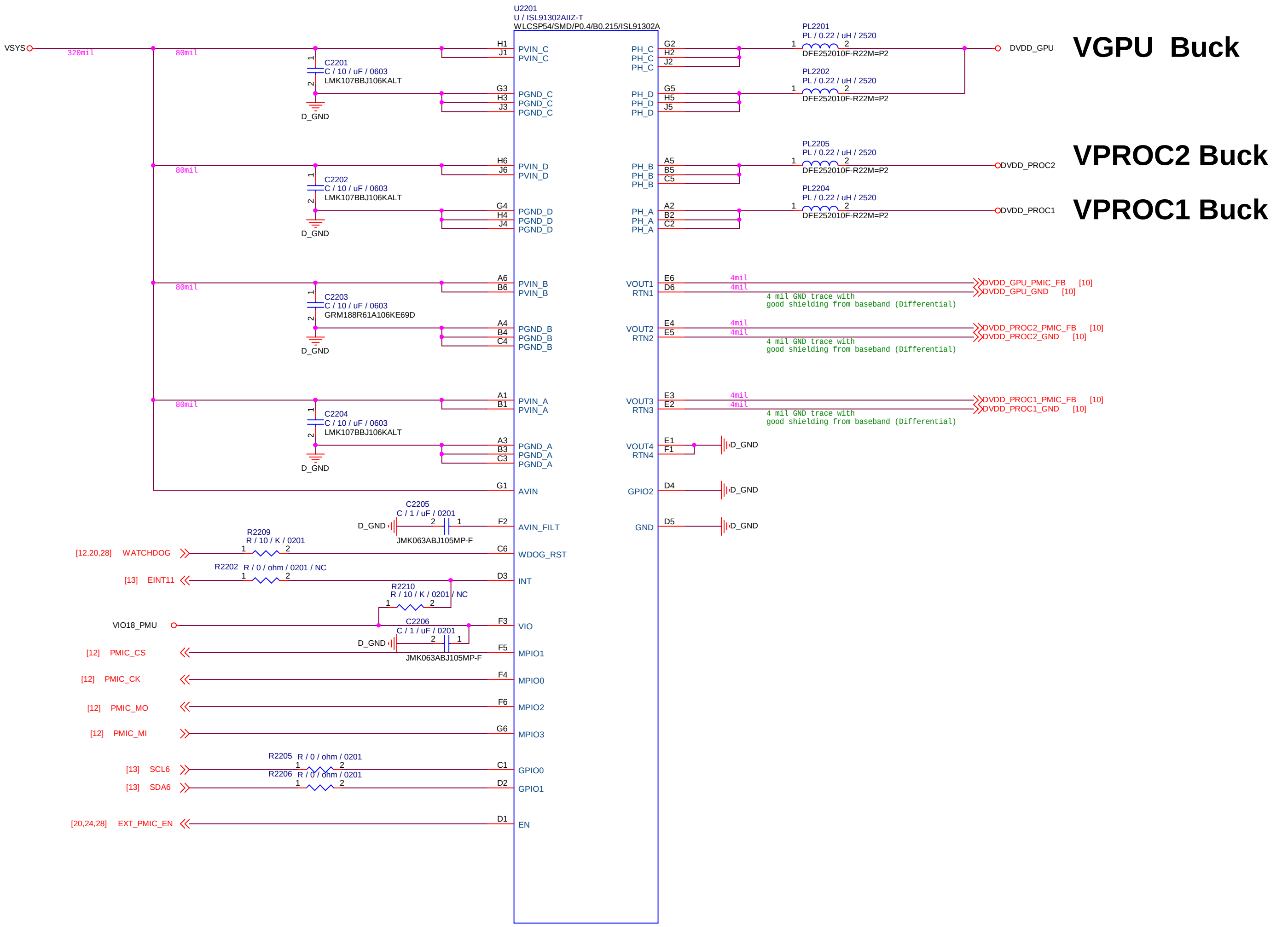
MEDIATEK

Title: 21_POWER_MT6335_2

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 | Sheet 21 of 99



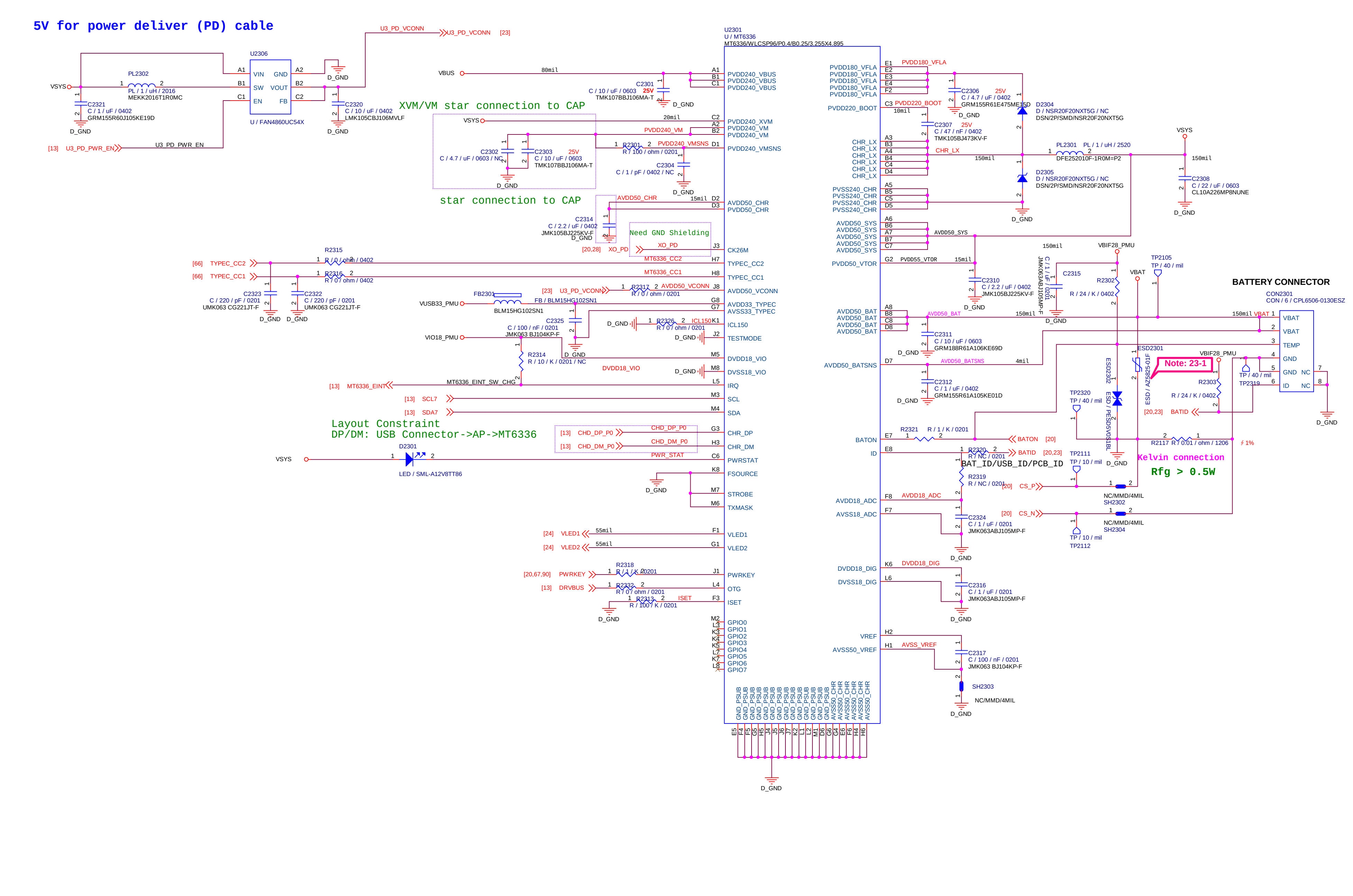
MEDIATEK

Title: 22_POWER_ISL91302A

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 | Sheet 22 of 99



Schematic design notice of "23_POWER_MT6336" page.

Note 23-1: For better ESD or surge performance we need choose suitable device for system protection. please refer to "Surge device selection guide V2.0" provide by MTK.

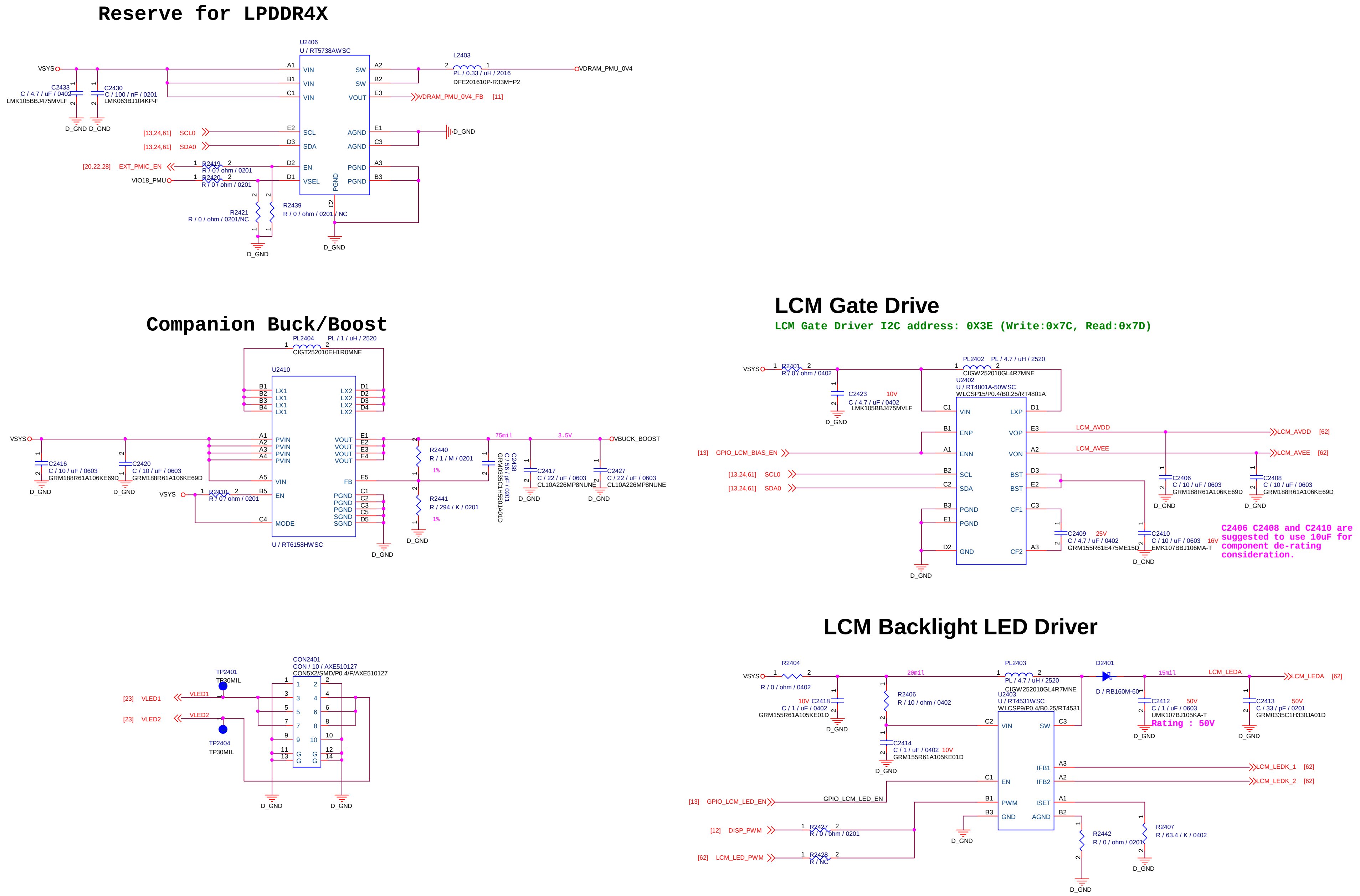
MEDIATEK

Title: 23_POWER_MT6336

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 23 of 99



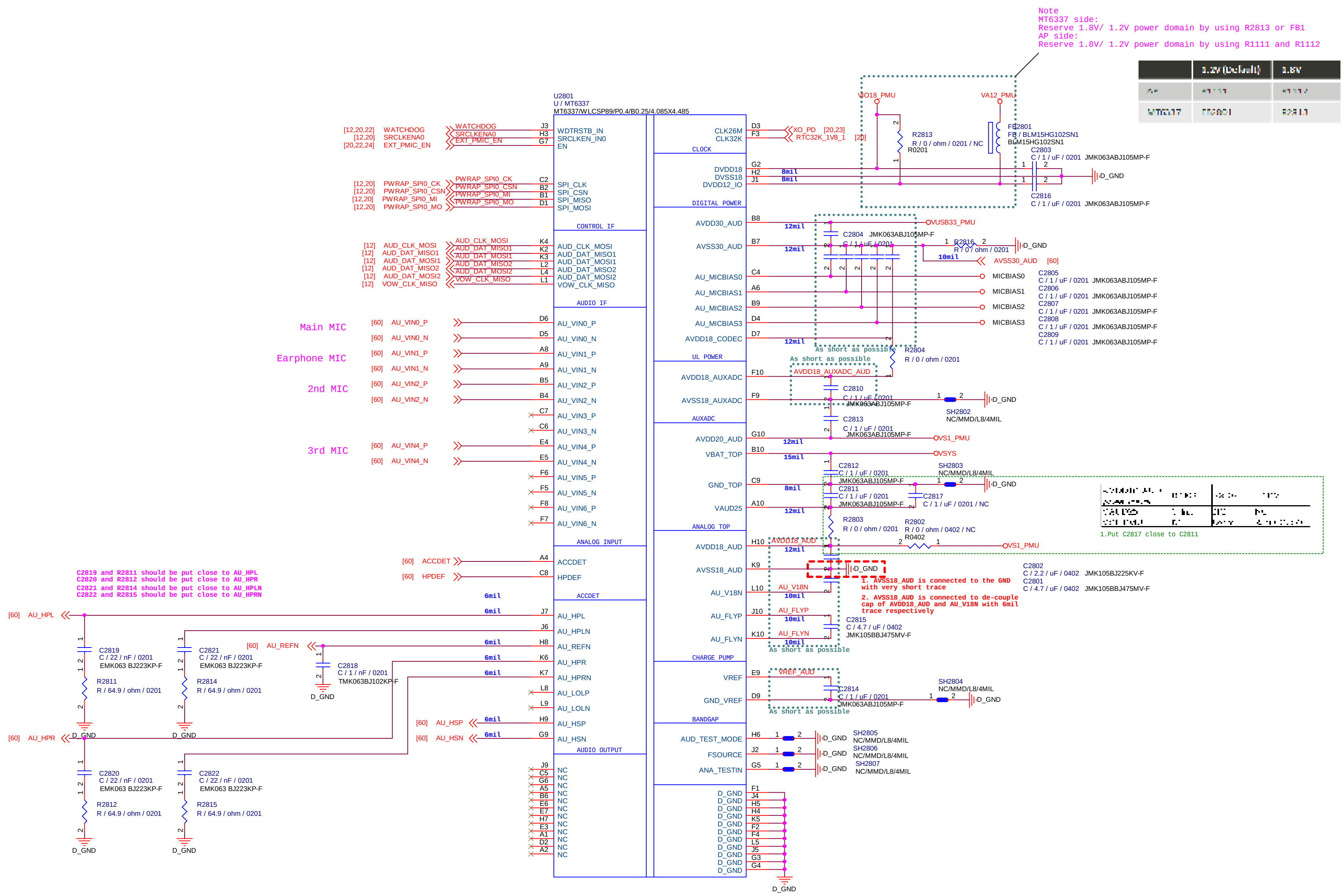
MEDIATEK

Title: 24_POWER_THIRD-PARTY

Size: C

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 24 of 99

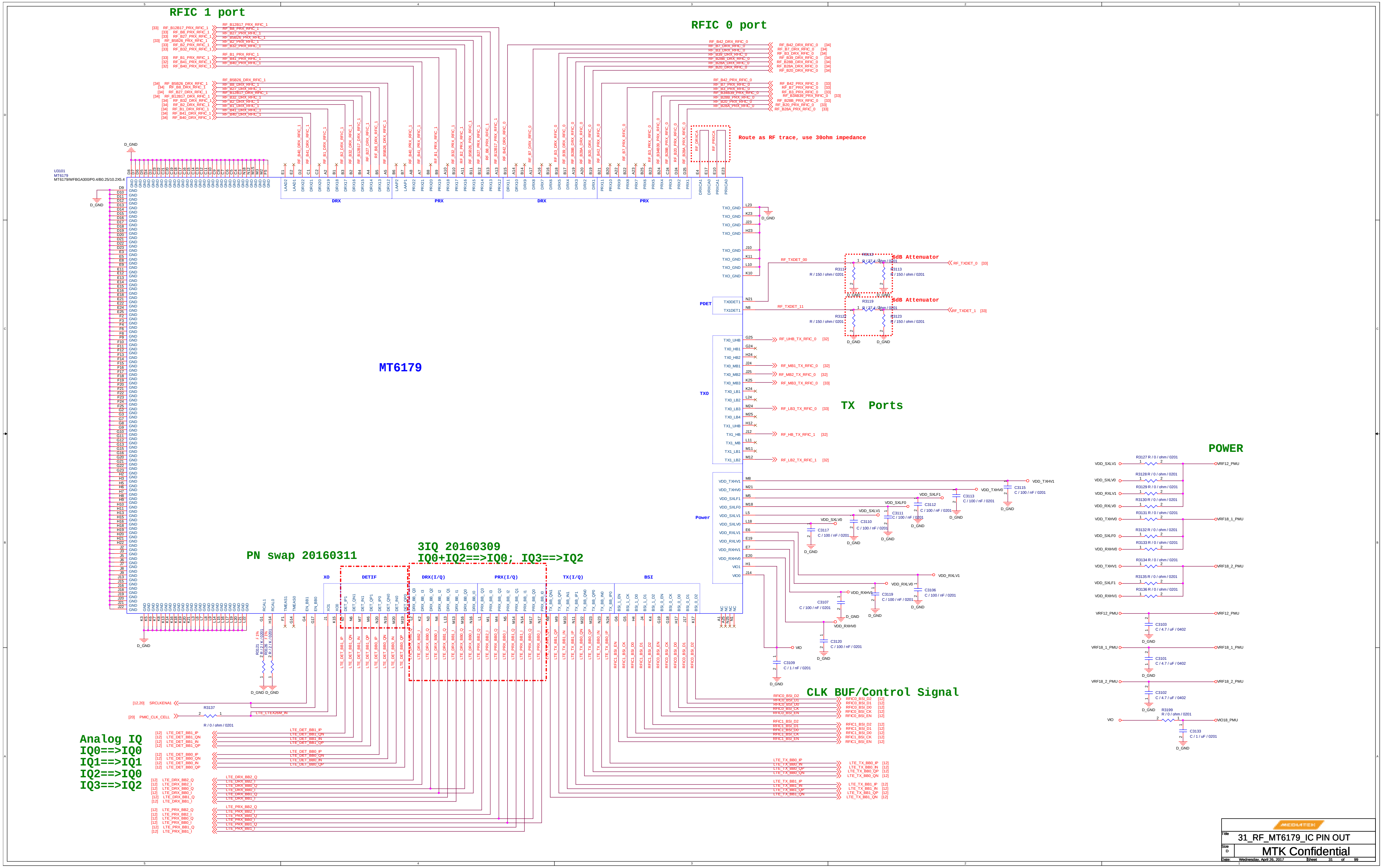


MEDIATEK

Title
28_AUDIO_MT6337

Size C
MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 28 of 99


RFIC 1 port
RFIC 0 port
Route as RF trace, use 30ohm impedance
6dB Attenuator
6dB Attenuator
MT6179
U3101
MT6179
MT6179/WFBGA300/P0.4/B0.25/10.2X5.4
TX Ports
POWER
PN swap 20160311
3IQ 20160309
IQ0+IQ2==>IQ0; IQ3==>IQ2
CLK BUF/Control Signal
Analog IQ
IQ0==>IQ0
IQ1==>IQ1
IQ2==>IQ0
IQ3==>IQ2
DRX
PRX
DRX
PRX
PDET
TXO
Power
XO
DETIF
DRX(I/Q)
PRX(I/Q)
TX(I/Q)
BSI
31_RF_MT6179_IC PIN OUT
MTK Confidential
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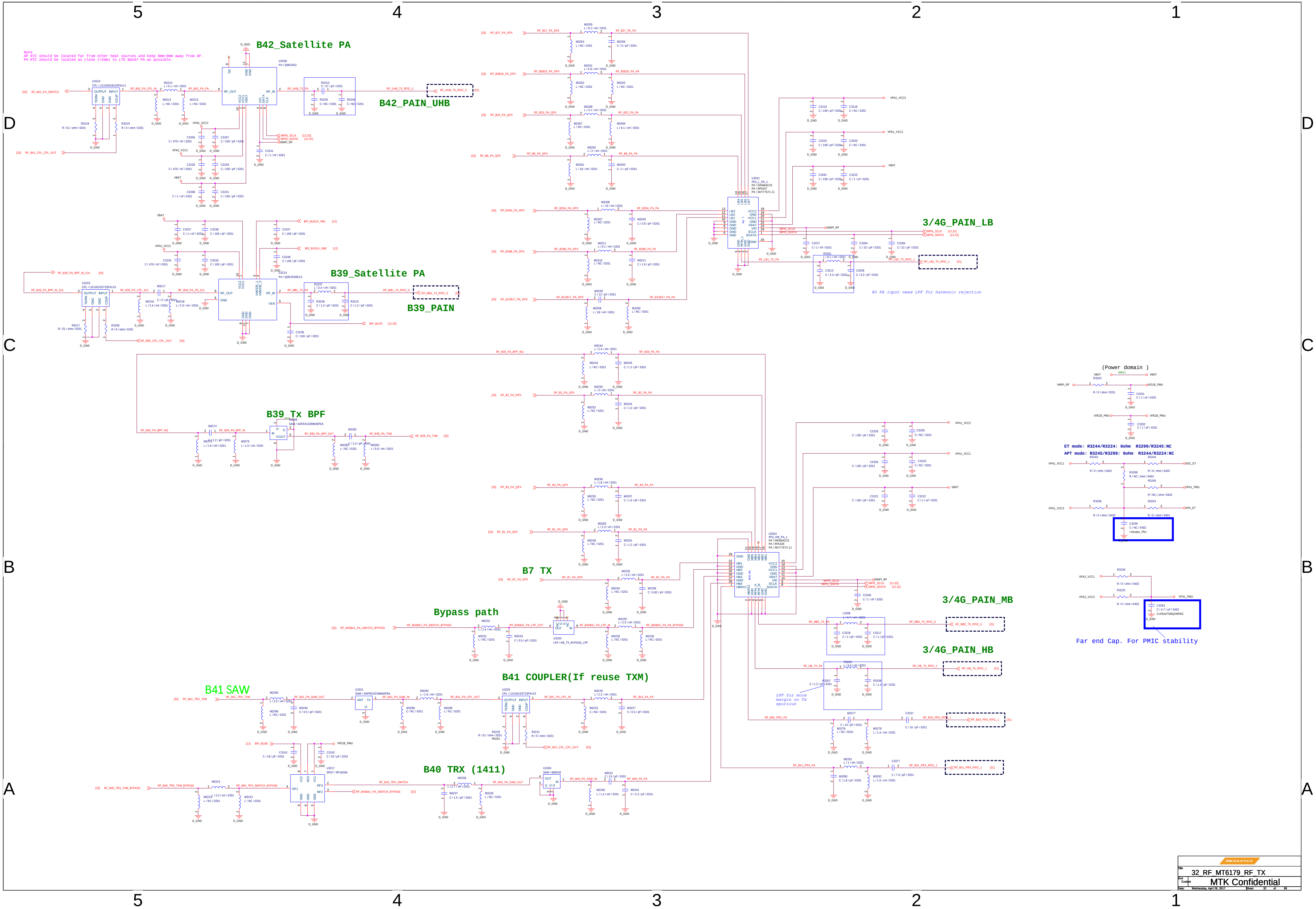
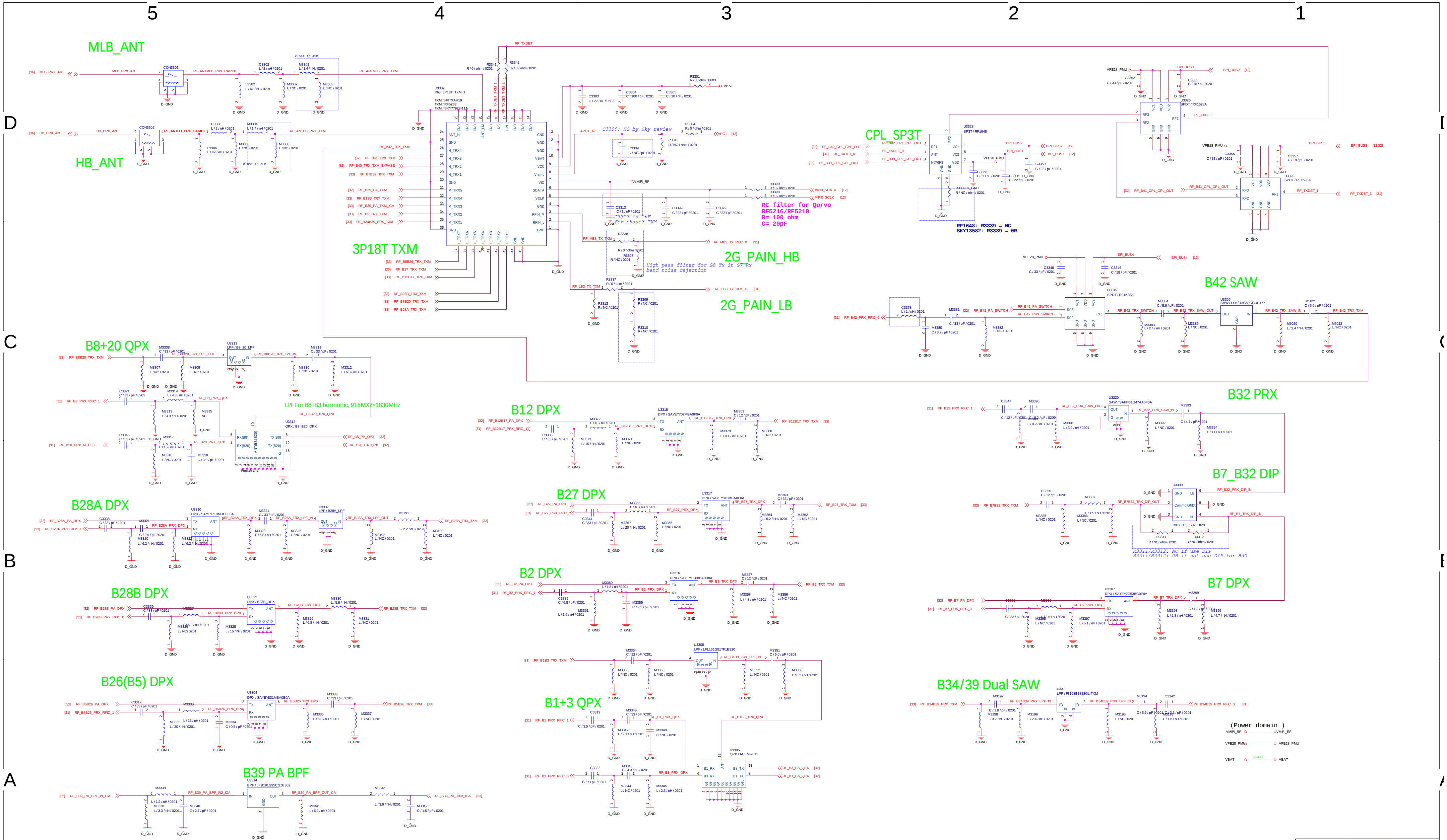

Note
AP NTC should be located far from other heat sources and keep 6mm~8mm away from AP.
PA NTC should be located as close (<2mm) to LTE Band7 PA as possible.
B42_Satellite PA
B42_PAIN_UHB
3/4G_PAIN_LB
4G PA input need LPF for harmonic rejection
B39_Satellite PA
B39_PAIN
B39_Tx BPF
(Power domain)
ET mode: R3244/R3224: 0ohm R3299/R3245:NC
APT mode: R3245/R3299: 0ohm R3244/R3224:NC
B7 TX
Bypass path
3/4G_PAIN_MB
3/4G_PAIN_HB
Far end Cap. For PMIC stability
LPF for more margin on Tx spurious
B41 COUPLER(If reuse TXM)
B41 SAW
B40 TRX (1411)
32_RF_MT6179_RF_TX
MTK Confidential
Wednesday, April 26, 2017



33_RF_MT6179_RF_PRX

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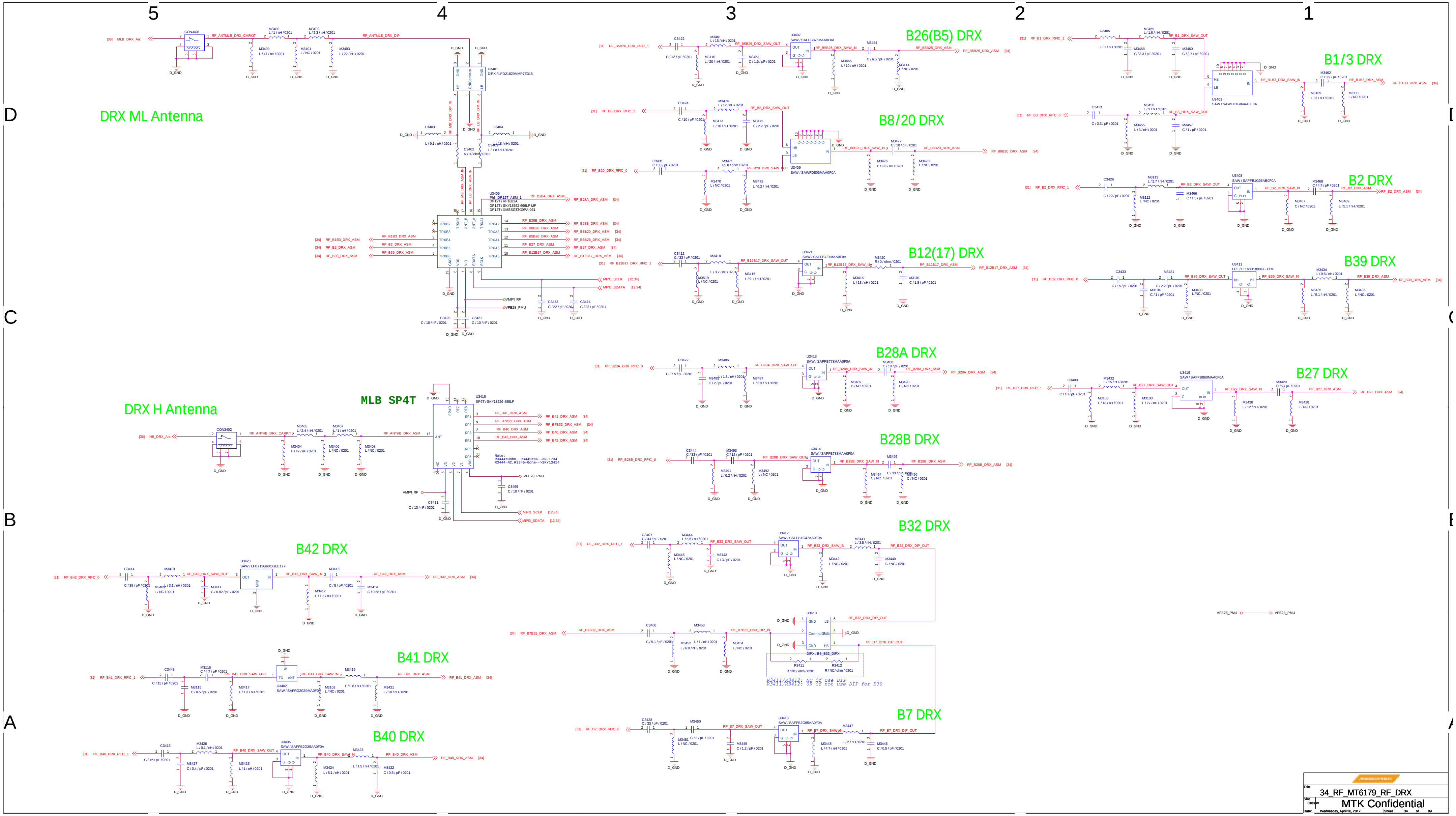
DRX ML Antenna
DRX H Antenna
MLB SP4T
B26(B5) DRX
B1/3 DRX
B8/20 DRX
B2 DRX
B12(17) DRX
B39 DRX
B28A DRX
B27 DRX
B28B DRX
B32 DRX
B42 DRX
B41 DRX
B40 DRX
B7 DRX
R3411/R3412: NC if use DIP
R3411/R3412: OR if not use DIP for B30
34_RF_MT6179_RF_DRX
MTK Confidential
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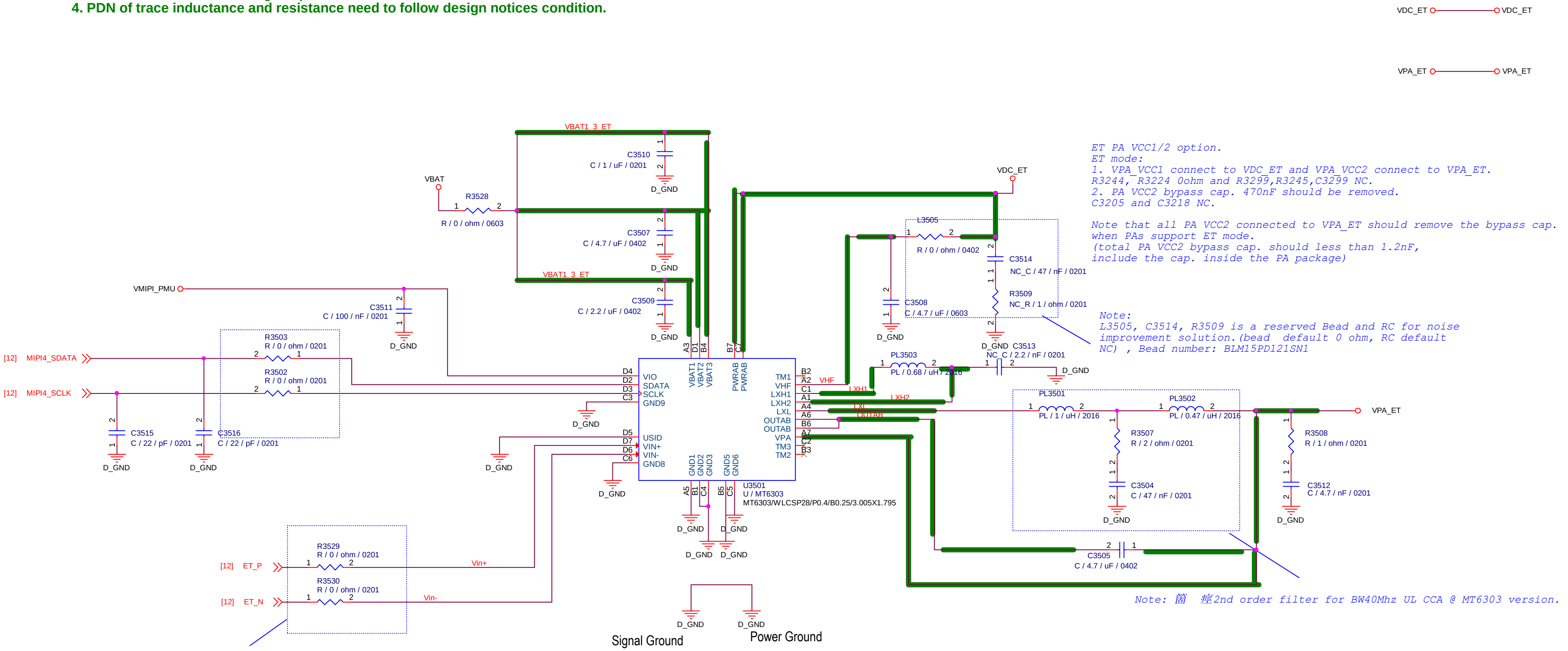
Envelope Tracking

MMD rule:
1. C3510, C3507 C3509 , C3508 need to placement as close as chip and follow MMD.
2. Power input trace need to through cap first than into IC ball.
3. GND need to connect through cap first than into main GND.
4. PDN of trace inductance and resistance need to follow design notices condition.



ET PA VCC1/2 option.
ET mode:
1. VPA_VCC1 connect to VDC_ET and VPA_VCC2 connect to VPA_ET.
R3244, R3224 0ohm and R3299,R3245,C3299 NC.
2. PA VCC2 bypass cap. 470nF should be removed.
C3205 and C3218 NC.

Note that all PA VCC2 connected to VPA_ET should remove the bypass cap.
when PAs support ET mode.
(total PA VCC2 bypass cap. should less than 1.2nF,
include the cap. inside the PA package)

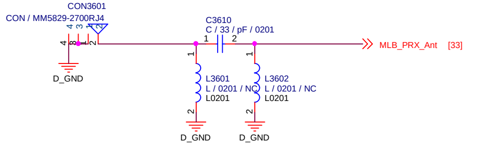
Note:
L3505, C3514, R3509 is a reserved Bead and RC for noise improvement solution.(bead default 0 ohm, RC default NC) , Bead number: BLM15PD121SN1

Note: 箇 瘦2nd order filter for BW40Mhz UL CCA @ MT6303 version.

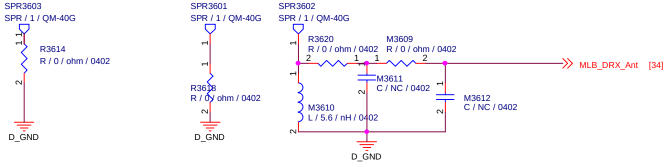
Note:
MT6300 ET differential input should connect to
MT6797 ball M4 and N4
ET_P connect to M4
ET_N connect to N4

Title	35_RF_ET
Size C	MTK Confidential
Date: Wednesday, April 26, 2017	Sheet 35 of 99

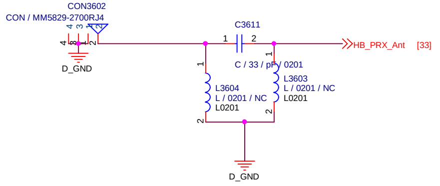
LB/MB PRX ANT Connector (ANT0_LM)



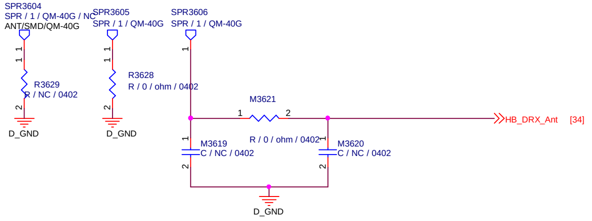
LB/MB DRX ANT (ANT1_LM)



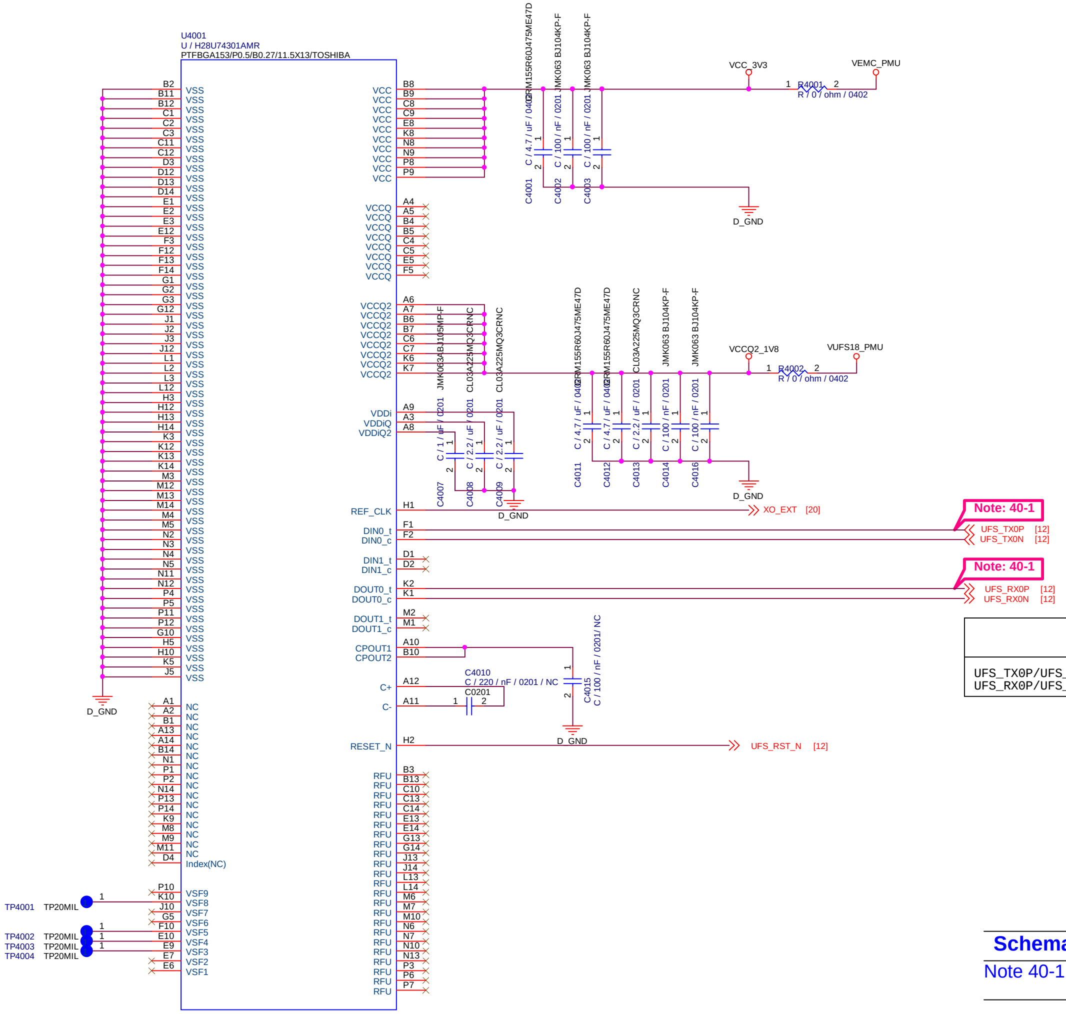
HB PRX ANT Connector (ANT0_H)



HB DRX ANT (ANT1_H)



Title	36_RF_ANT
Size C	MTK Confidential
Date: Wednesday, April 26, 2017	Sheet 36 of 99



	Differential impedance	P/N length skew	Total length	Number of vias allowed
UFS_TX0P/UFS_TX0N UFS_RX0P/UFS_RX0N	100 ohm	< 5 mil	< 6 inches	< 2 (0 is better)

Schematic design notice of "40_MEMORY_UFS" page.

Note 40-1: Customer must control differential impedance to 100 ohm by their PCB stack-up.
Differential pairs are well-shielded by GND (adjacent and up/down layers).

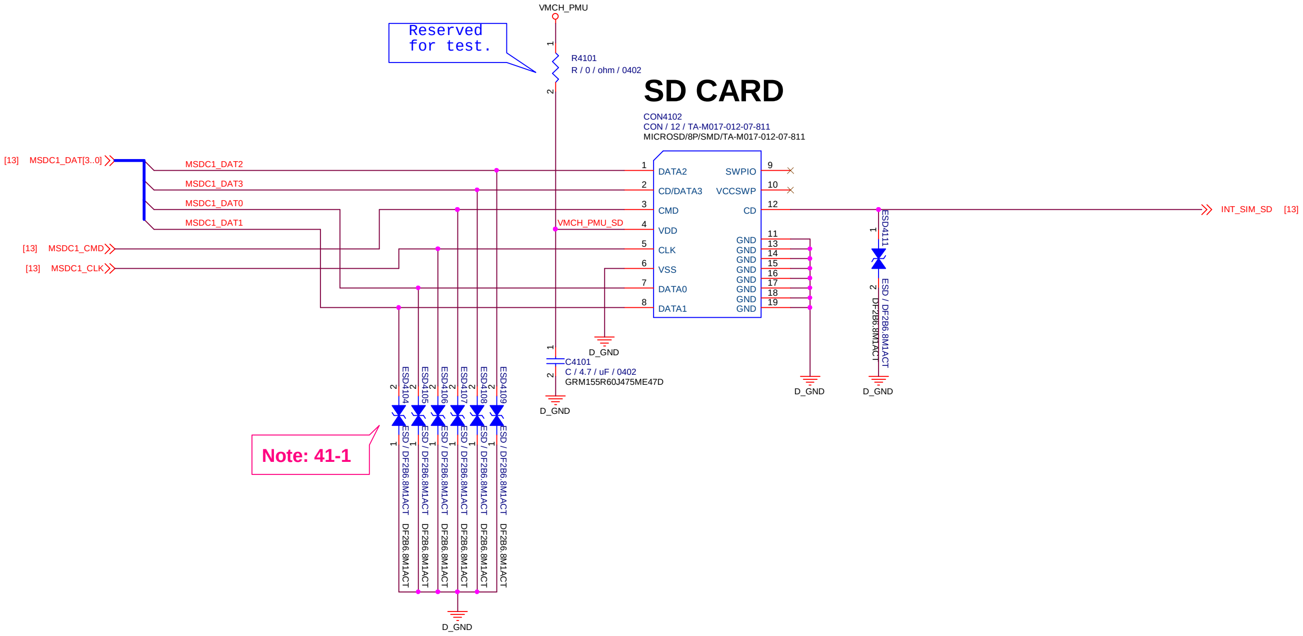
MEDIATEK

Title: 40_MEMORY_UFS

Size: C

MTK Confidential

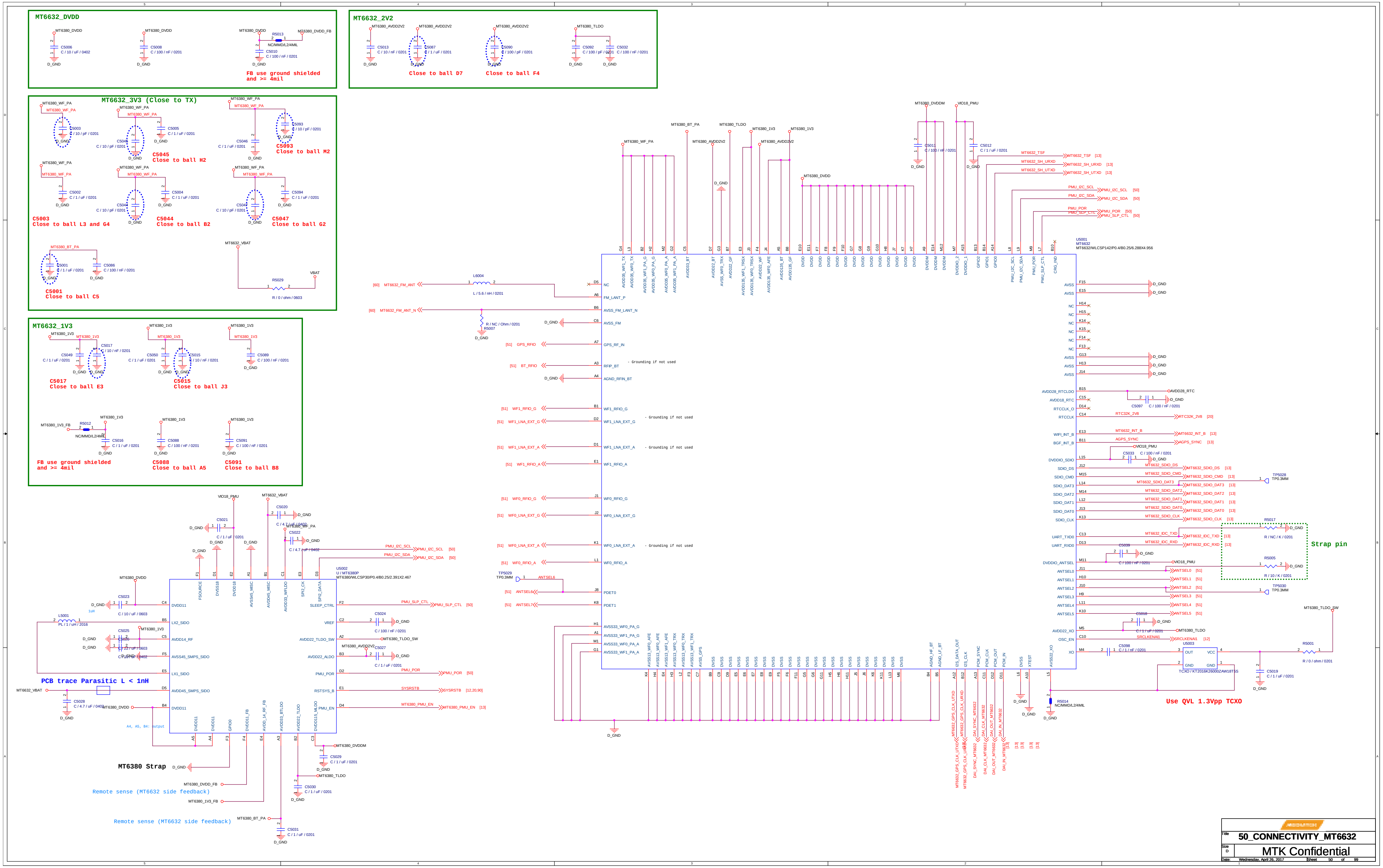
Date: Wednesday, April 26, 2017 Sheet 40 of 99



Schematic design notice of "41_MEMORY_SD Card" page.

Note 41-1: Depends on system design to add ESD protection componemt or not.

Title	41_MEMORY_SD Card
Size C	MTK Confidential
Date: Wednesday, April 26, 2017	Sheet 41 of 99

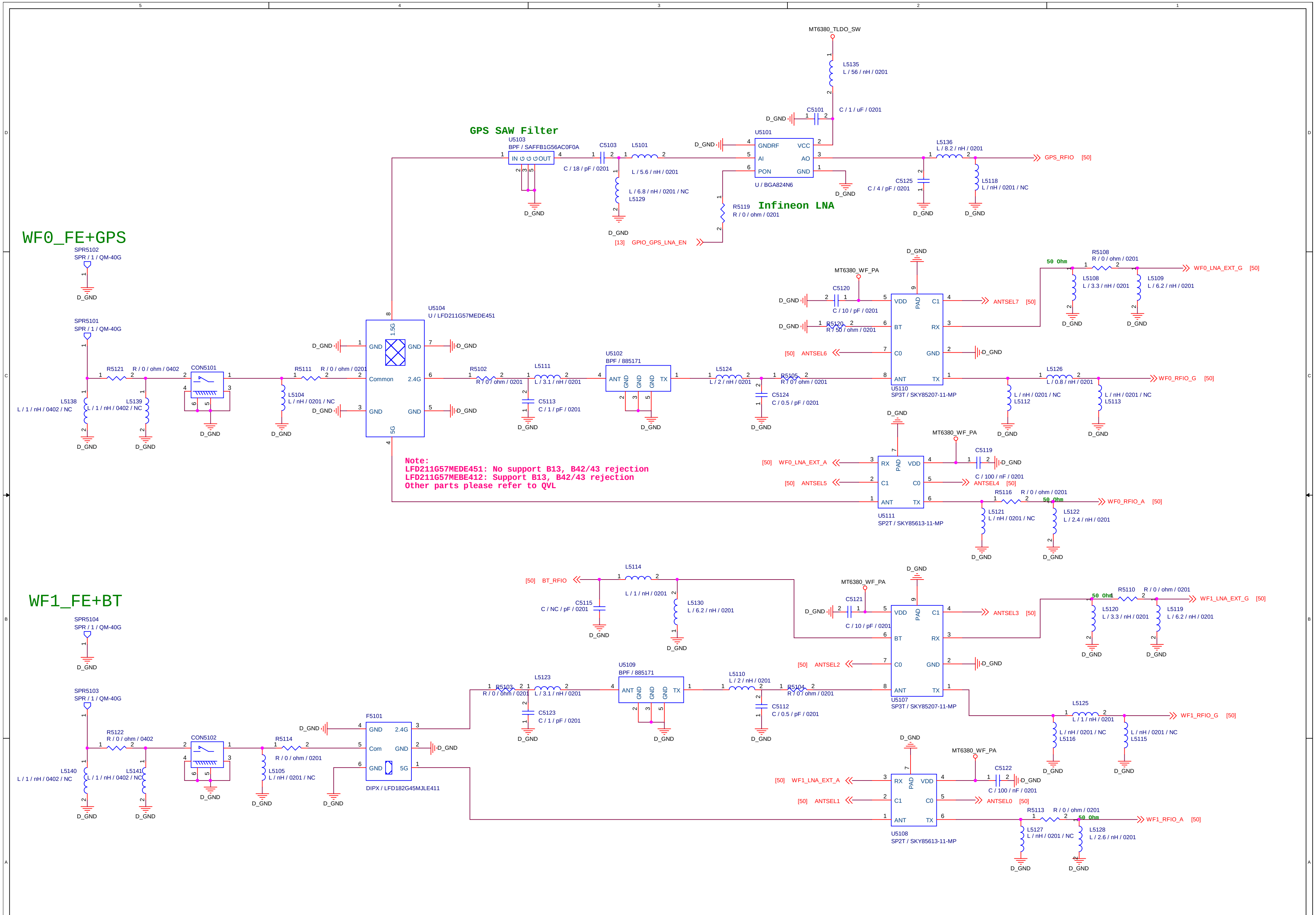


Title: 50_CONNECTIVITY_MT6632

Size: D

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 50 of 99



MEDIATEK

Title 51_CONNECTIVITY_MT6632_RF_FE

Size C

MTK Confidential

Date: Wednesday, April 26, 2017 Sheet 51 of 99

Traces in below region need well GND shielding

MT6605 sol. and MT6605 ACFD sol.
1. L5201=L5202=560nH; R5234=R5231=0
2. R5229=U5207=R5230=R5232=R5233=R5248=NC; C5219=180pF; R5209=7.5K

MT6605+AS39230 sol.
1. L5201=L5202=R5234=R5231=NC; R5229=R5230=R5233=R5248=0
2. U5207=NTNUS3171PZT5G; C5219=0.1uF; R5209=2K; R5232=3.9K

1. Please choose QVL low parasitic, low threshold voltage PMOS
2. R5248 is reserved for card mode performance tuning

EMI filter LC value is 5% accuracy at least.

MT6605 EMI filter

R5215/C5237 are close to each other

MT6605 sol.
1. C5222=R5235=NC
2. R5212=0

MT6605 ACFD sol.
1. R5235=NC
2. C5222=4.7uF, R5212=10K

MT6605+AS39230 sol.
1. R5235=0
2. R5212=C5222=NC

SYSRST_B (NFC_RST)
1. Input pin
2. Internal pull high
3. Low active

OSC_EN (NFC_OSC_EN)
1. NFC_OSC_EN is output pin, and high active.
2. Need to connect to host SRCLKENAI and SRCLKENAI pin need to be default low.

1. MT6605 I2C address is 0x28
2. MT6605 can't support SW I2C and only HW I2C is allowed
3. C5234, C5235 are for I2C signal rise/fall time adjustment if necessary

R5205 NC : XTAL MODE
R5205 10K : Co-Clock

1. L5201, L5202, C5204, C5218, C5233, R5209, R5231, R5232, R5233 are close to MT6605 IC.
2. C5205, C5214, C5203, C5207 are close to MT6605 IC
3. L5201, L5202 must be MTK QVL parts

IRQ (NFC_IRQ)
1. IRQ is output pin and high active
2. IRQ is also a NFC strap pin
3. Host EINT connected with IRQ must be default low

EINT (NFC_EINT)
1. Input pin
2. Internal pull low
3. High active

Please must reserve TP5201 ~ TP5210 for debug

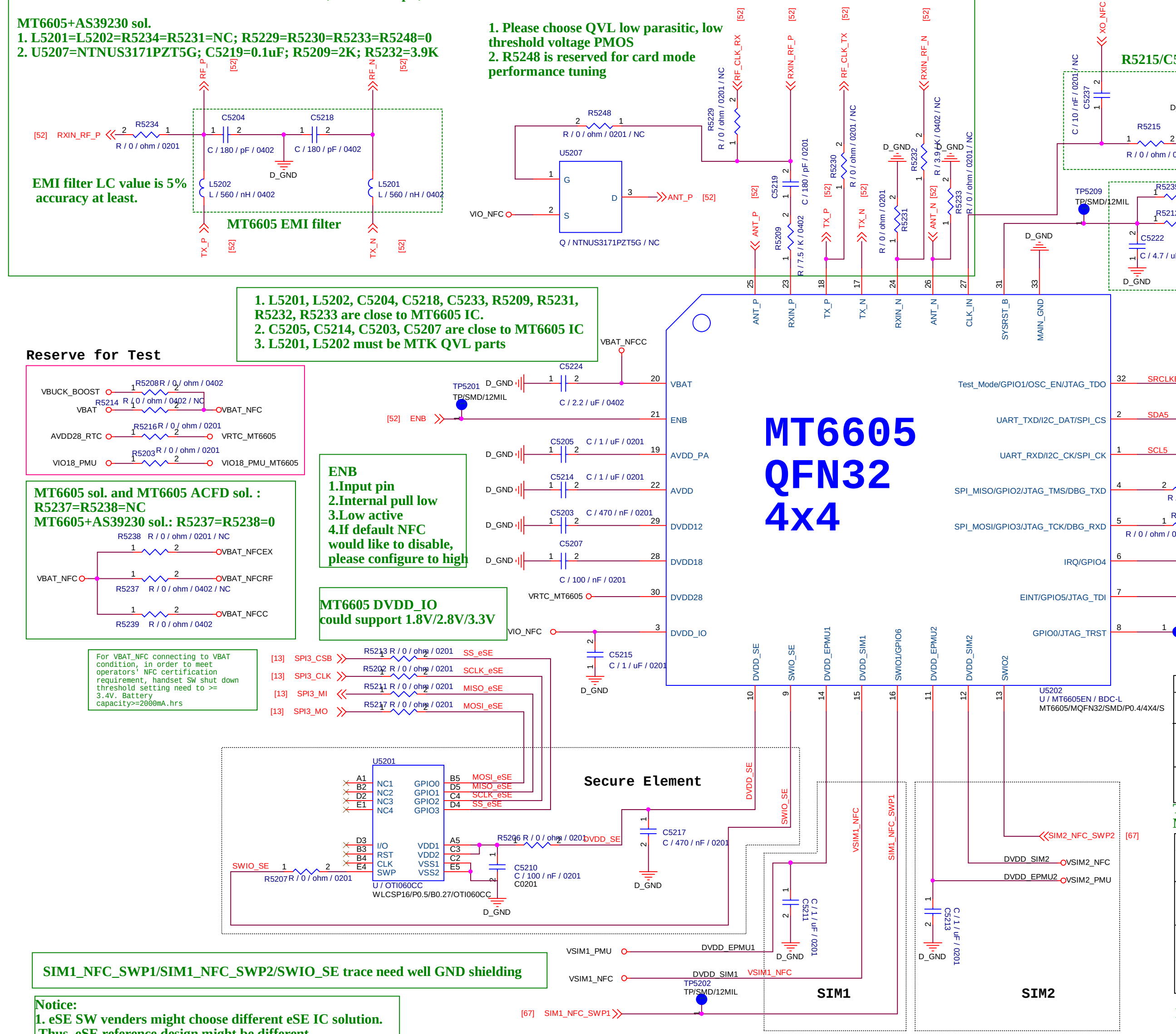
Reserve for Test

MT6605 sol. and MT6605 ACFD sol. :
R5237=R5238=NC
MT6605+AS39230 sol.: R5237=R5238=0

ENB
1. Input pin
2. Internal pull low
3. Low active
4. If default NFC would like to disable, please configure to high

MT6605 DVDD_IO could support 1.8V/2.8V/3.3V

For VBAT_NFC connecting to VBAT condition, in order to meet operators' NFC certification requirement, handset SW shut down threshold setting need to >= 3.4V. Battery capacity>=2000mA.hrs



SIM1_NFC_SWP1/SIM1_NFC_SWP2/SWIO_SE trace need well GND shielding

Notice:
1. eSE SW venders might choose different eSE IC solution. Thus, eSE reference design might be different
2. Customer must confirm eSE reference design with eSE SW venders if the eSE P/N is not MTK suggested
3. Customers should contact eSE SW venders for eSE SW Ver. and eSE IC shipment
4. The qualified eSE list are shown in MTK eSE QVL

TX output inductor QVL for MT6605+AS39230 sol.

Vender	Type	Size	Value	P/N	Accuracy	DCR	Rated Current
TDK	Multilayer	0402	75nH	MLJ1005W75NJ	?5%	0.2ohm ?30%	550mA
TDK	Multilayer	0402	82nH	MLJ1005W82NJ	?5%	0.14ohm ?30%	600mA
Murata	Wire Wound	0402	75nH	LQW15AN75NG80	?5%	1.224ohm Max.	320mA

TX output inductor QVL for MT6605 sol. and MT6605 ACFD sol.

Vender	Type	Size	Value	P/N	Accuracy	DCR	Rated Current
TDK	Multilayer	0603	560nH	MLJ1608WR56J	?5%	0.4ohm ?30%	400mA
TDK	Multilayer	0603	560nH	MLF1608DR56J	?5%	1.05ohm ?30%	100mA
TDK	Multilayer	0402	560nH	MLJ1005WR56J	?5%	1.08ohm ?30%	250mA
Murata	Multilayer	0603	560nH	LQB18NNR56J10D	?5%	0.85ohm Max.	300mA

POWER MODE[1:0]=[SYSRST_B:ENB] for MT6605 sol. and MT6605 ACFD sol.

Power Mode	NFC_RST	NFC_VENB	VIO_NFC	SYSRST_B	ENB
Full power suspend	1	1	1	1	1
NFC enable (configure, R/W, card, polling loop, full power standby)	1	0	1	1	0
NFC disable (HPD)	0	1	1	0	1
Reset	0	0	1	0	0

POWER MODE[1:0]=[SYSRST_B:ENB] for MT6605+AS39230 sol.

Power Mode	NFC_RST	NFC_VENB	VIO_NFC	SYSRST_B	ENB
Full power suspend	0	0	1	1	1
NFC enable (configure, R/W, card, polling loop, full power standby)	1	0	1	1	0
NFC disable (HPD)	0	1	0	0	1

MEDIATEK

Title: 52_CONNECTIVITY_NFC_MT6605

Size: C — MTK Confidential

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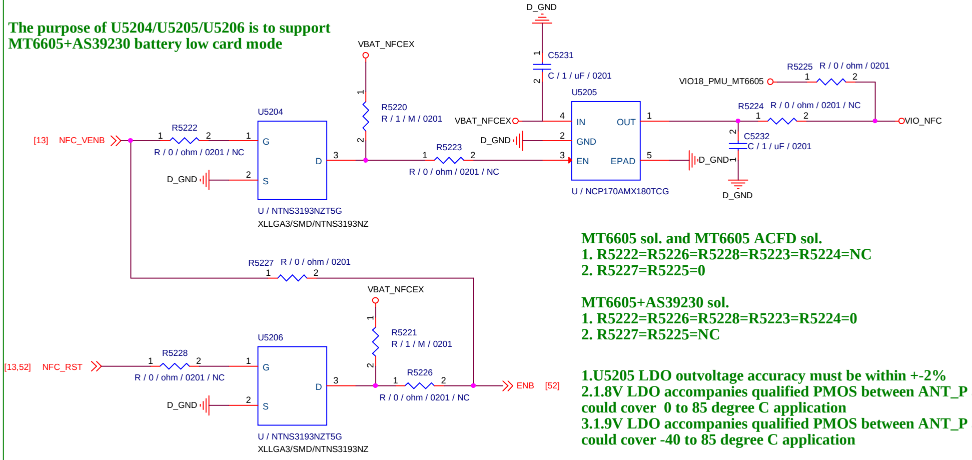
The purpose of U5204/U5205/U5206 is to support MT6605+AS39230 battery low card mode



MT6605 sol. and MT6605 ACFD sol.
1. R5222=R5226=R5228=R5223=R5224=NC
2. R5227=R5225=0

MT6605+AS39230 sol.
1. R5222=R5226=R5228=R5223=R5224=0
2. R5227=R5225=NC

1.U5205 LDO outvoltage accuracy must be within +-2%
2.1.8V LDO accompanies qualified PMOS between ANT_P anD RF_CLK_RX could cover 0 to 85 degree C application
3.1.9V LDO accompanies qualified PMOS between ANT_P anD RF_CLK_RX could cover -40 to 85 degree C application

NFC sol.	Host GPIO	MT6605 GPIO	Host GPIO default setting in DWS file	Host GPIO setting in DTS file
MT6605 sol.	NFC_VENB	ENB	Output High	NFC_VENB =High-->MT6605 ENB=High NFC_VENB=Low-->MT6605 ENB=Low
	NFC_RST	SYSRST_B	Output Low	NFC_RST=High-->MT6605 SYSRST_B=High NFC_RST=Low-->MT6605 SYSRST_B=Low
MT6605 ACFD sol.	NFC_VENB	ENB	Output High	NFC_VENB =High-->MT6605 ENB=High NFC_VENB=Low-->MT6605 ENB=Low
	NFC_RST	SYSRST_B	Output Low	NFC_RST=High-->MT6605 SYSRST_B=High NFC_RST=Low-->MT6605 SYSRST_B=Low
MT6605+AS39230 sol.	NFC_VENB	SYSRST_B	Output Low	NFC_VENB =High-->MT6605 SYSRST_B=Low NFC_VENB=Low-->MT6605 SYSRST_B=High
	NFC_RST	ENB	Output Low	NFC_RST=High-->MT6605 ENB=Low NFC_RST=Low-->MT6605 ENB=High

Recommended NFC antenna spec. for MT6605 sol. and MT6605 ACFD sol.
1. La @ 1MHZ is 2 ~ 2.5uH
2. Rs,dc @1MHZ < 2ohm
3. Fra_ant > 25MHZ
4. Antenna Q > 20

Recommended NFC antenna spec. for MT6605+AS39230 sol.
1. La @ 13.56MHZ is 0.2uH ~ 0.6uH
2. Fra_ant > 30MHZ
3. Antenna Q> 20
4. Antenna turns: 2~6 turns

NFC_VENB and NFC_RSTmust be internal default pull low for MT6605+AS39230 sol

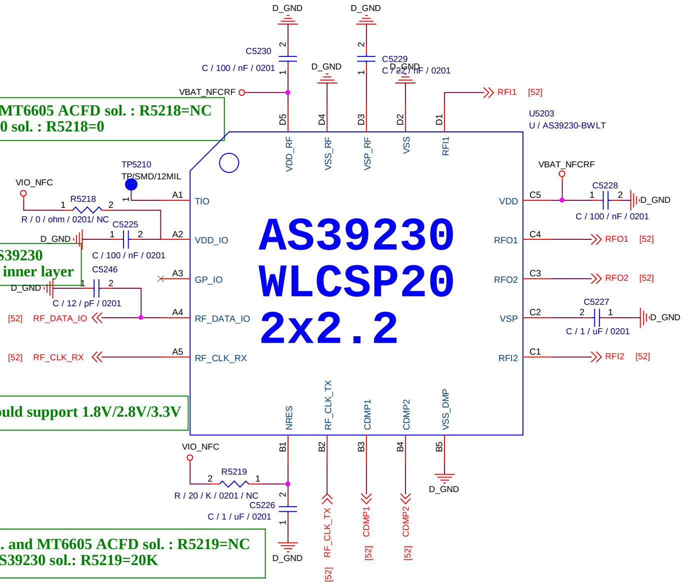
Below RF traces need well GND shielding

MT6605 sol. and MT6605 ACFD sol.
1. L5203=L5204=C5236=C5221=C5238=R5204=R5240=C5241=C5240=R5244=R5246=NC
2. Matching network: C5201,C5202,C5239,C5209,C5206,C5223,C5208,C5242,C5244,C5243, C5245
3. Damping resistor: R5247

MT6605+AS39230 sol.
1. L5203=L5204=75nH; C5236=C5221=560pF; R5204=R5240=R5246=R5244=0
2. C5238=R5241=R5242=C5241=C5206=C5223=R5243=R5245=NC; C5240=1nF
3. Matching network: C5201,C5202,C5239,C5209,C5208,C5242,C5244,C5243,C5245
4. Damping resistor: R5247

The purpose of damping resistor is
1. To control network Q within 20~35 for MT6605 sol. and MT6605 ACFD sol.
2. To control network Q~15 for MT6605+AS39230 sol.

MT6605 sol. and MT6605 ACFD sol. : R5218=NC
MT6605+AS39230 sol. : R5218=0

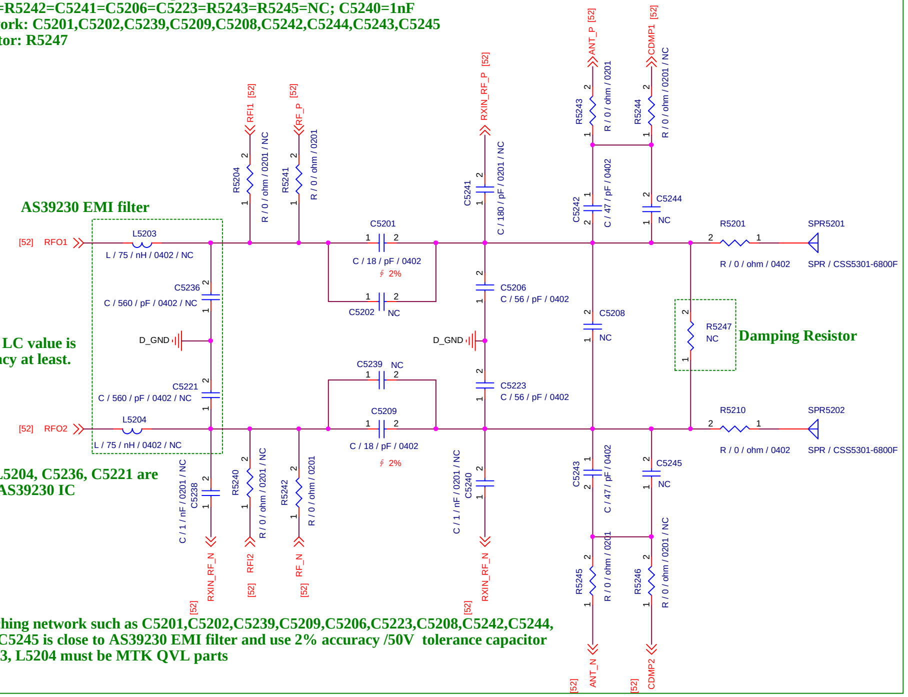


1. C5246 close to AS39230
2. Data_IO route in inner layer

AS39230 IO voltage could support 1.8V/2.8V/3.3V

MT6605 sol. and MT6605 ACFD sol. : R5219=NC
MT6605+AS39230 sol.: R5219=20K

RF_CLK_RX and RF_CLK_TX traces need well GND shielding



EMI filter LC value is 5% accuracy at least.

Damping Resistor

L5203, L5204, C5236, C5221 are close to AS39230 IC

1. Matching network such as C5201,C5202,C5239,C5209,C5206,C5223,C5208,C5242,C5244, C5243,C5245 is close to AS39230 EMI filter and use 2% accuracy /50V tolerance capacitor
2. L5203, L5204 must be MTK QVL parts

MEDIATEK

Title: 52_CONNECTIVITY_NFC_FE

Size: C

MTK Confidential

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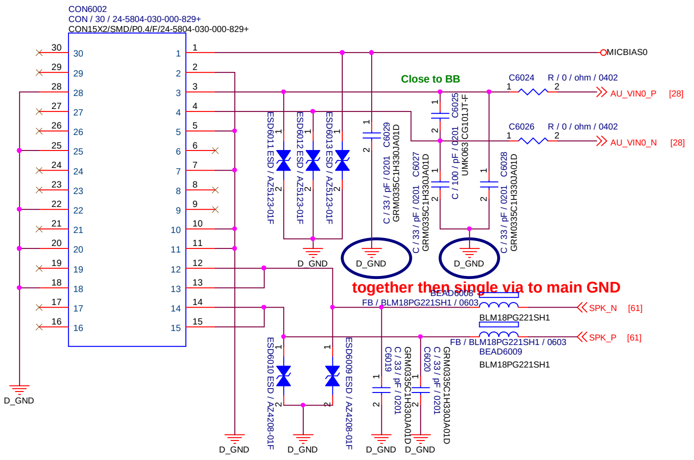
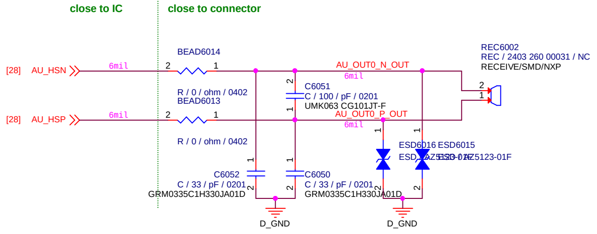
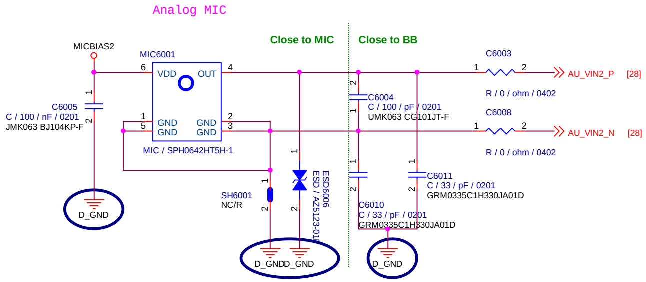
Audio/Speech DTB I/F + Handset 1st microphone (in the bottom)



Receiver

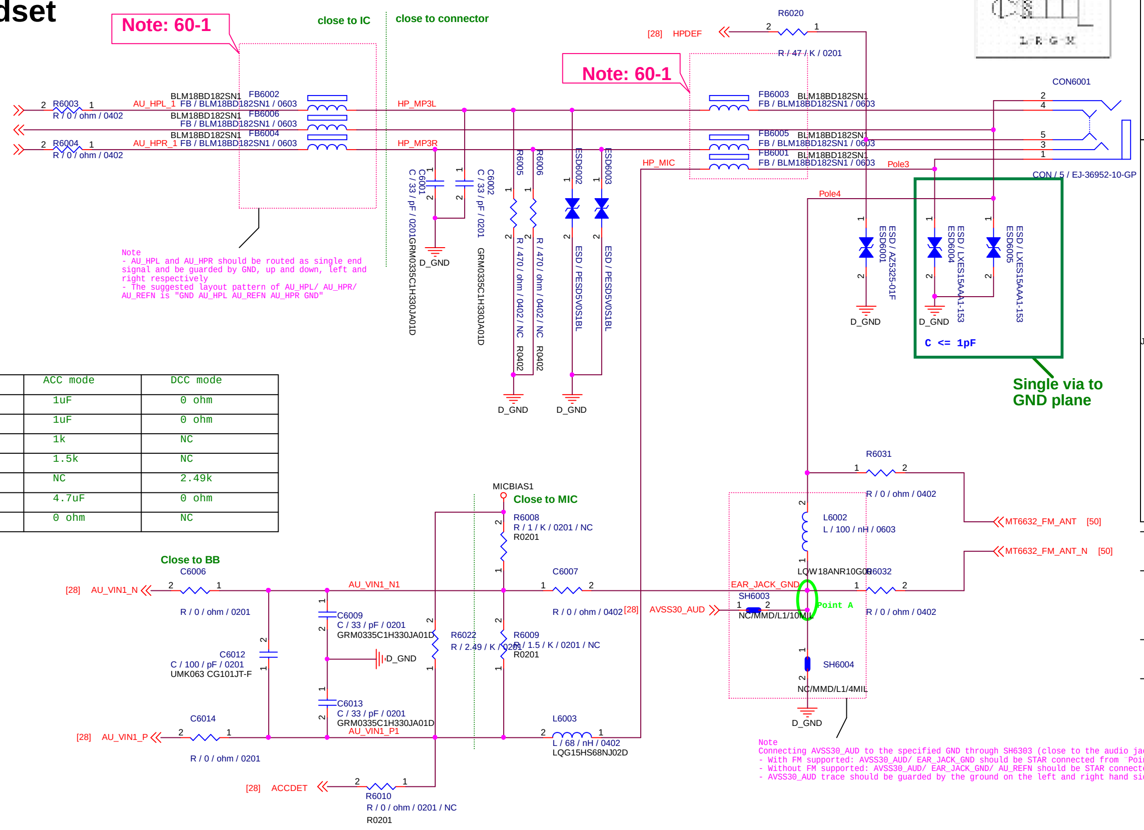


Handset 2nd microphone (in the back)



Headset

Note: 60-1

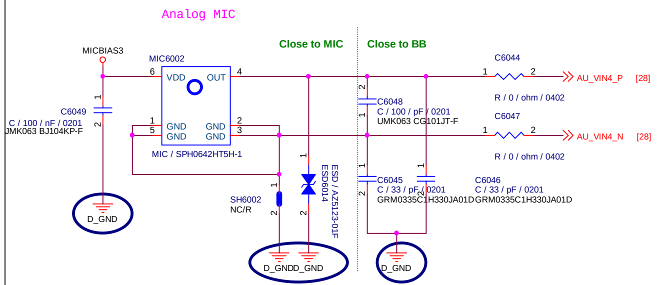


Note
- AU_HPL and AU_HPR should be routed as single end signal and be guarded by GND, up and down, left and right respectively
- The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN is "GND AU_HPL AU_REFN AU_HPR GND"

	ACC mode	DCC mode
C6006	1uF	0 ohm
C6014	1uF	0 ohm
R6008	1k	NC
R6009	1.5k	NC
R6022	NC	2.49k
C6007	4.7uF	0 ohm
C6010	0 ohm	NC

Note
Connecting AVSS30_AUD to the specified GND through SH6303 (close to the audio jack) with 10mil trace
- With FM supported: AVSS30_AUD/ EAR_JACK_GND should be STAR connected from "Point A" with >10mil (Green path)/ 4mil trace respectively
- Without FM supported: AVSS30_AUD/ EAR_JACK_GND/ AU_REFN should be STAR connected from "Point A" with >10mil (Green path)/ 4mil/ 6mil trace respectively
- AVSS30_AUD trace should be guarded by the ground on the left and right hand side and kept away from the high power/ switching signal

Handset 3rd microphone (close to receiver)



Schematic design notice of "60_PERI_AUDIO_IO" page.

Note 60-1: Part # of FB6002, FB6003, FB6004 and FB6005 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 60-2: MIPI0 I/F is reserved for CLAT (Closed-loop-antenna-tuner)

MEDIATEK

Title: 60_PERI_AUDIO_IO

Size: C

MTK Confidential

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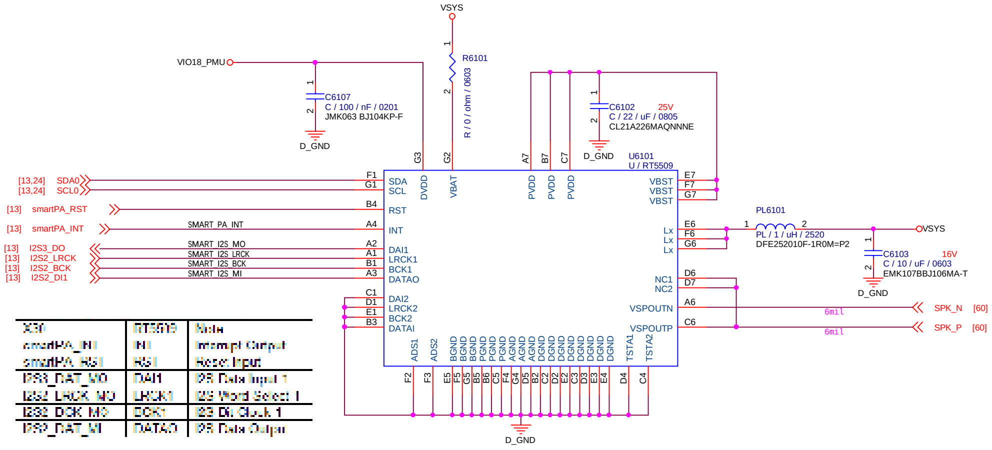
Speaker Amplifier



X30	RT5509	Note
smartPA_INT	INT	Interrupt Output
smartPA_RST	RST	Reset Input
I2S3_DAT_MO	DAI1	I2S Data Input 1
I2S2_LRCK_MO	LRCK1	I2S Word Select 1
I2S2_BCK_MO	BCK1	I2S Bit Clock 1
I2S2_DAT_MI	DATAO	I2S Data Output

Title: 61_PERI_SPEAKER_AMP

Size: C

MTK Confidential

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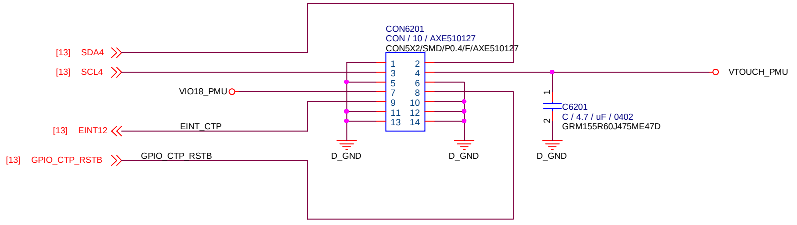
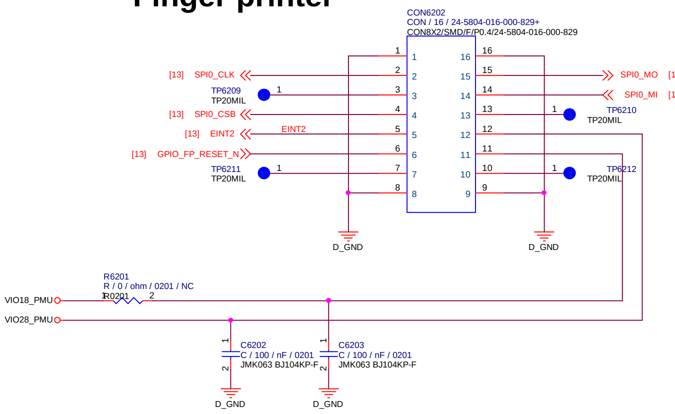
CTP

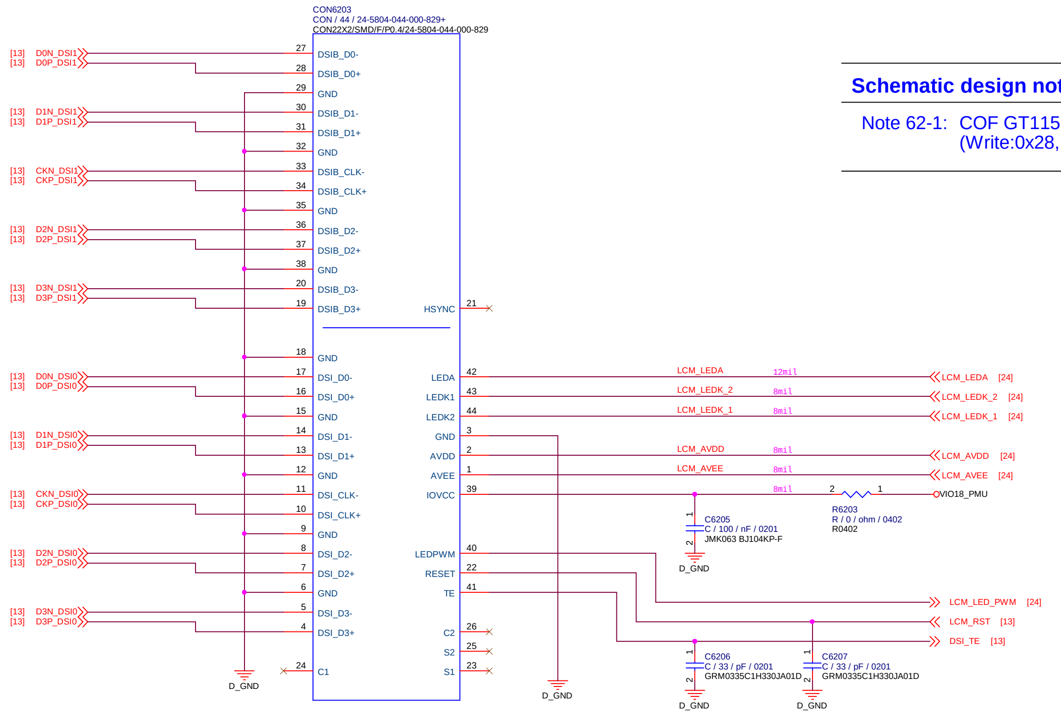
GT1511 / CTPI2C address: 0X5D (Write:0xBA, Read:0xBB)
GT1511 / CTPI2C address: 0X14 (Write:0x28, Read:0x29)



Finger printer



Main LCM

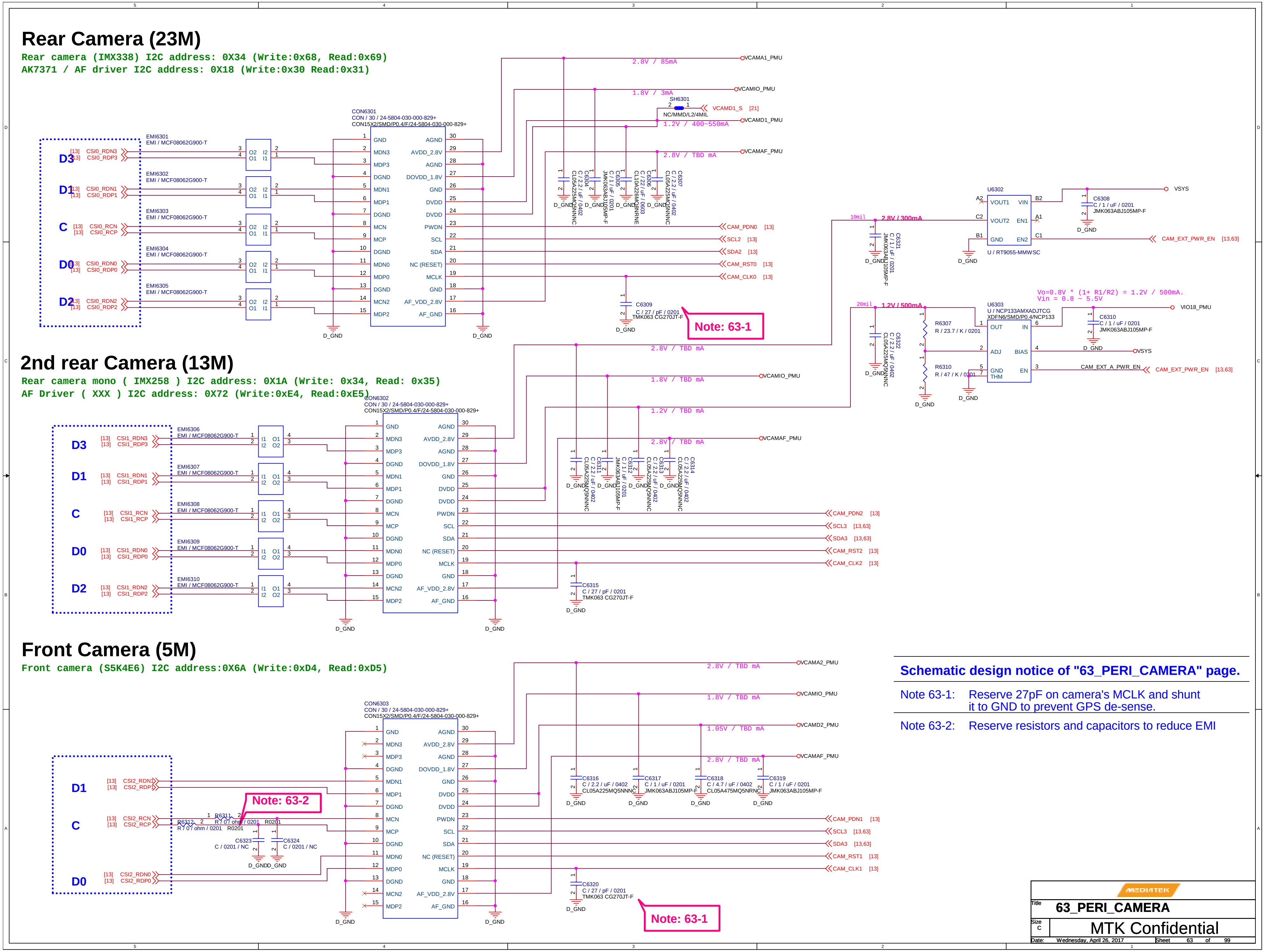


Schematic design notice of "62_PERI_LCD_CTP" page.

Note 62-1: COF GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB) Or, 0X14 (Write:0x28, Read:0x29)

MEDIATEK

Title	62_PERI_LCD_CTP
Size C	MTK Confidential
Date: Wednesday, April 26, 2017	Sheet 62 of 99


Rear Camera (23M)
Rear camera (IMX338) I2C address: 0X34 (Write:0x68, Read:0x69)
AK7371 / AF driver I2C address: 0X18 (Write:0x30 Read:0x31)
CON6301
CON / 30 / 24-5804-030-000-829+
CON15X2/SMD/P0.4/F/24-5804-030-000-829+
2.8V / 85mA
VCAMA1_PMU
1.8V / 3mA
VCAMIO_PMU
SH6301
NC/MMD/L2/4MIL
VCAMD1_S [21]
1.2V / 400~550mA
VCAMD1_PMU
2.8V / TBD mA
VCAMAF_PMU
EMI6301
EMI / MCF08062G900-T
CSI0_RDN3
CSI0_RDP3
CSI0_RDN1
CSI0_RDP1
CSI0_RCN
CSI0_RCP
CSI0_RDN0
CSI0_RDP0
CSI0_RDN2
CSI0_RDP2
CAM_PDN0 [13]
SCL2 [13]
SDA2 [13]
CAM_RST0 [13]
CAM_CLK0 [13]
C6309
C / 27 / pF / 0201
TMK063 CG270JT-F
Note: 63-1
D_GND
U6302
U / RT9055-MMWSC
2.8V / 300mA
VSYS
C6308
C / 1 / uF / 0201
JMK063ABJ105MP-F
CAM_EXT_PWR_EN [13,63]
U6303
U / NCP133AMXADJTCG
XDFN6/SMD/P0.4/NCP133
Vo=0.8V * (1+ R1/R2) = 1.2V / 500mA.
Vin = 0.8 ~ 5.5V
1.2V / 500mA
VIO18_PMU
R6307
R / 23.7 / K / 0201
R6310
R / 47 / K / 0201
C6310
C / 1 / uF / 0201
JMK063ABJ105MP-F
CAM_EXT_A_PWR_EN
CAM_EXT_PWR_EN [13,63]
2nd rear Camera (13M)
Rear camera mono (IMX258) I2C address: 0X1A (Write: 0x34, Read: 0x35)
AF Driver (XXX) I2C address: 0X72 (Write:0xE4, Read:0xE5)
CON6302
CON / 30 / 24-5804-030-000-829+
CON15X2/SMD/P0.4/F/24-5804-030-000-829+
2.8V / TBD mA
1.8V / TBD mA
VCAMIO_PMU
1.2V / TBD mA
2.8V / TBD mA
VCAMAF_PMU
CSI1_RDN3
CSI1_RDP3
CSI1_RDN1
CSI1_RDP1
CSI1_RCN
CSI1_RCP
CSI1_RDN0
CSI1_RDP0
CSI1_RDN2
CSI1_RDP2
CAM_PDN2 [13]
SCL3 [13,63]
SDA3 [13,63]
CAM_RST2 [13]
CAM_CLK2 [13]
C6315
C / 27 / pF / 0201
TMK063 CG270JT-F
Front Camera (5M)
Front camera (S5K4E6) I2C address:0X6A (Write:0xD4, Read:0xD5)
CON6303
CON / 30 / 24-5804-030-000-829+
CON15X2/SMD/P0.4/F/24-5804-030-000-829+
2.8V / TBD mA
VCAMA2_PMU
1.8V / TBD mA
VCAMIO_PMU
1.05V / TBD mA
VCAMD2_PMU
2.8V / TBD mA
VCAMAF_PMU
CSI2_RDN1
CSI2_RDP1
CSI2_RCN
CSI2_RCP
CSI2_RDN0
CSI2_RDP0
Note: 63-2
R6311
R / 0 / ohm / 0201
R6312
R / 0 / ohm / 0201
C6323
C / 0201 / NC
C6324
C / 0201 / NC
C6316
C / 2.2 / uF / 0402
CL05A225MQ5NNNC
C6317
C / 1 / uF / 0201
JMK063ABJ105MP-F
C6318
C / 4.7 / uF / 0402
CL05A475MQ5NRNC
C6319
C / 1 / uF / 0201
JMK063ABJ105MP-F
CAM_PDN1 [13]
SCL3 [13,63]
SDA3 [13,63]
CAM_RST1 [13]
CAM_CLK1 [13]
C6320
C / 27 / pF / 0201
TMK063 CG270JT-F
Note: 63-1
Schematic design notice of "63_PERI_CAMERA" page.
Note 63-1: Reserve 27pF on camera's MCLK and shunt it to GND to prevent GPS de-sense.
Note 63-2: Reserve resistors and capacitors to reduce EMI
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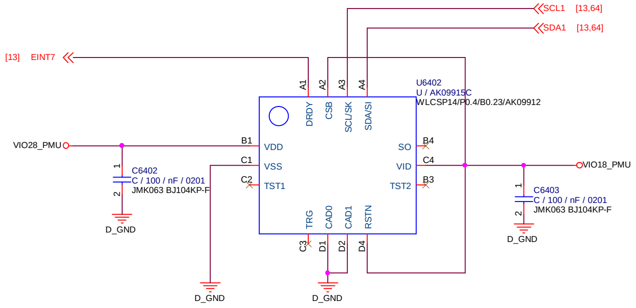
M-Sensor

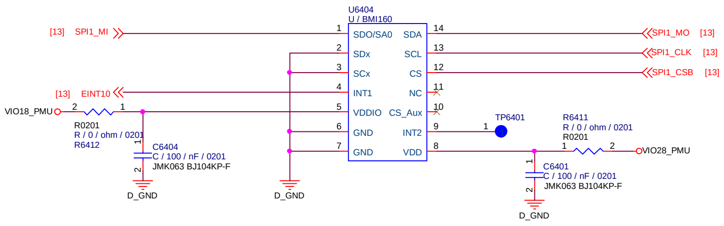
AK09915 / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)



Schematic design notice of "64_PERI_SENSORS" page.

Note 64-1: Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail

Accerometer + Gyro Sensor



Schematic design notice of "64_PERI_SENSORS" page.

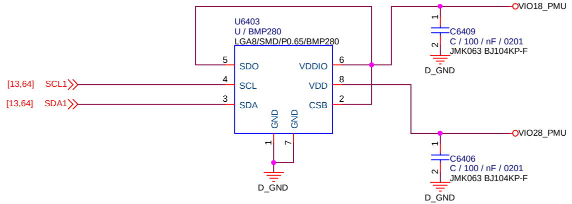
Note 64-2: For optmized GPS performance, please check HW design notice for Sensor selection guide

Note 64-3: MUST use SPI for optmized sensor hub performance
DO NOT USE I2C

Note 64-4: Suggest choose sensor support : FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.

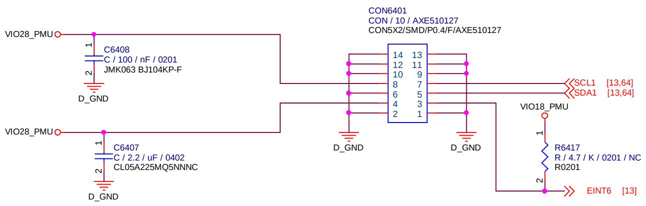
Baro Sensor

BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)

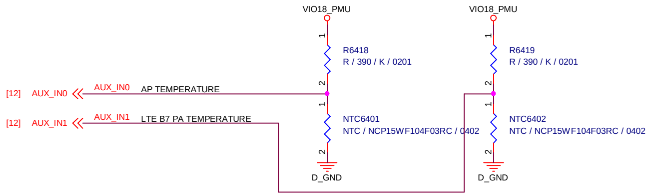


Light & Proximity Sensor

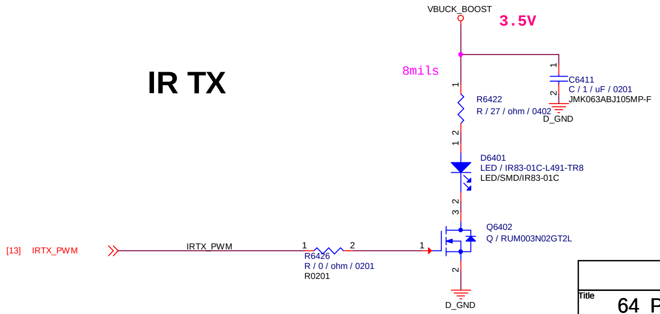
CM36558 / ALPS+UV I2C address: 0X51 (Write:0xA2, Read:0xA3)



Thermistor / To sense board level temperature



IR TX



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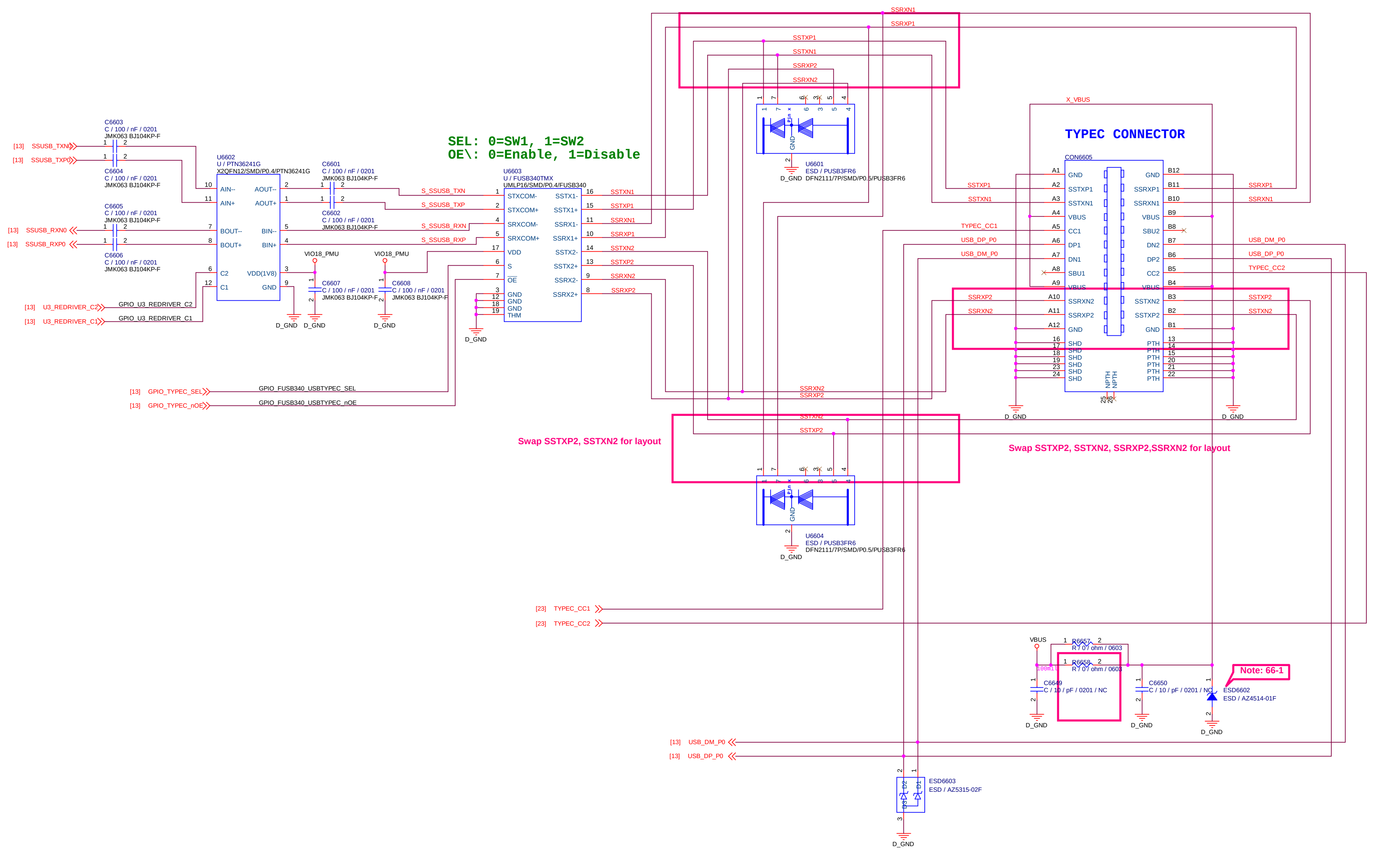

Schematic design notice of "66_PERI_USB_TYPEC" page.

Note 66-1: For better ESD or surge performance we need choose suitable device for system protection. please refer to ¨Surge device selection guide V2.0〃 provide by MTK.

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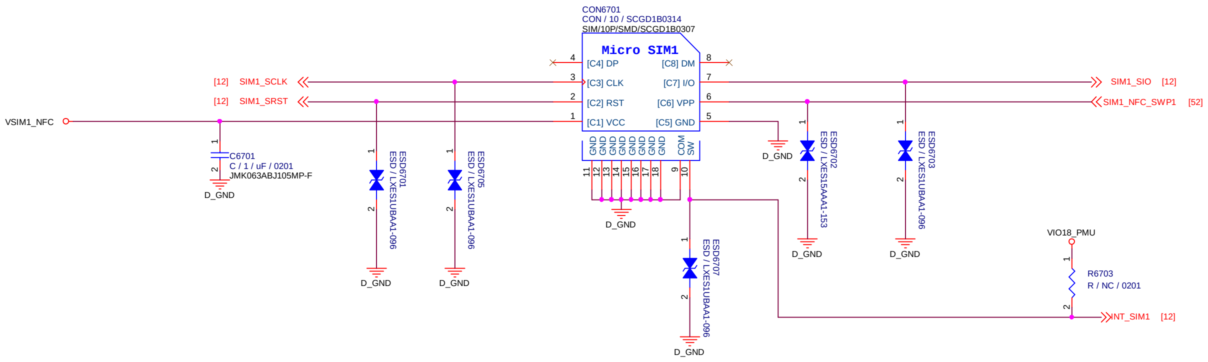
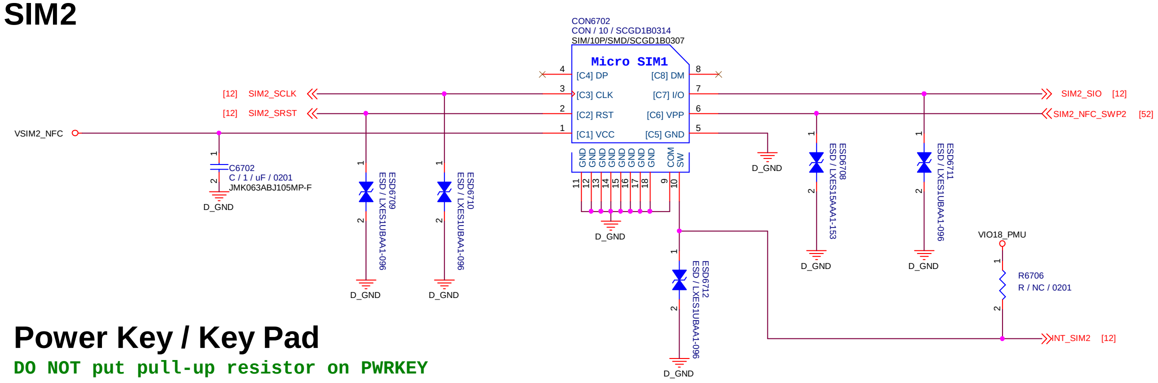
SIM1 & SmartCard

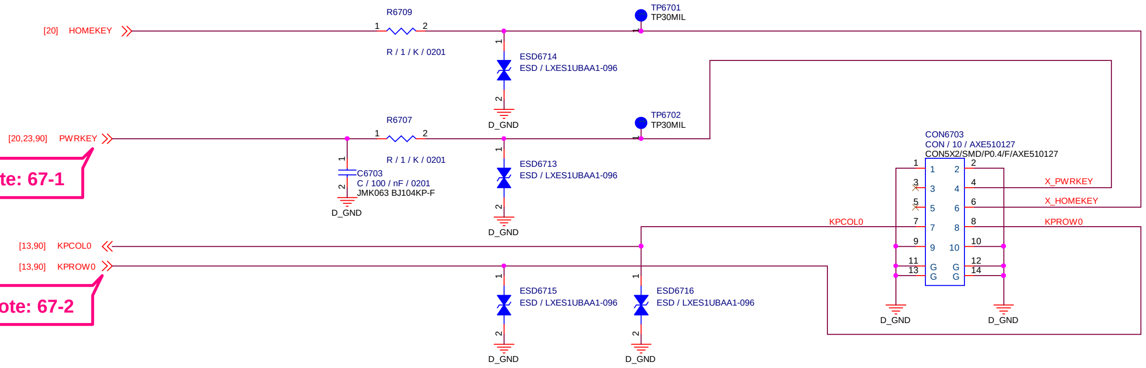


SIM2

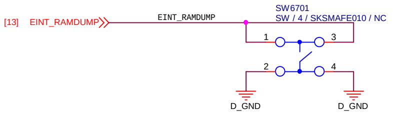


Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY



RAM dump key or test pin



Schematic design notice of "67_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 67-1:	DO NOT put pull-up resistor on PWRKEY
Note 67-2:	Volume Up : HOME Key / GND Volume Down : (KPROW0/KPCOL0) or KPCOL0 / GND

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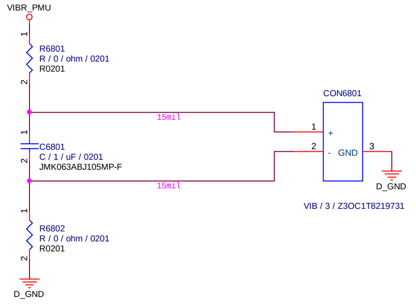
VIBRATOR



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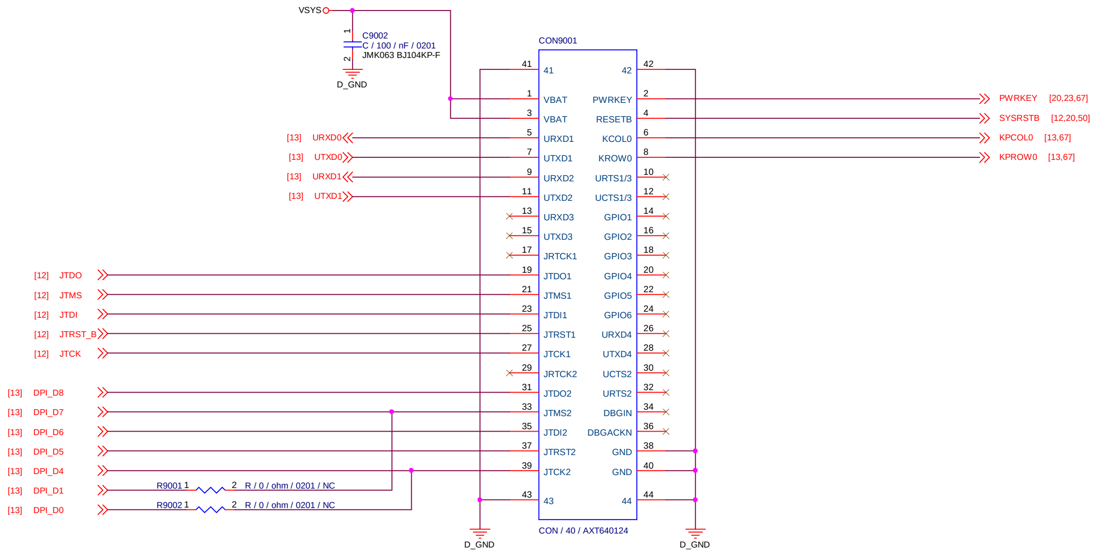
MTK Debug I/O



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Title: 90_DEBUG_IO

Size: C

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